2.830J / 6.780J / ESD.63J Control of Manufacturing Processes (SMA 6303)
Spring 2008

Control of Manufacturing Processes

Subject 2.830/6.780/ESD.63

Spring 2008

Lecture #2

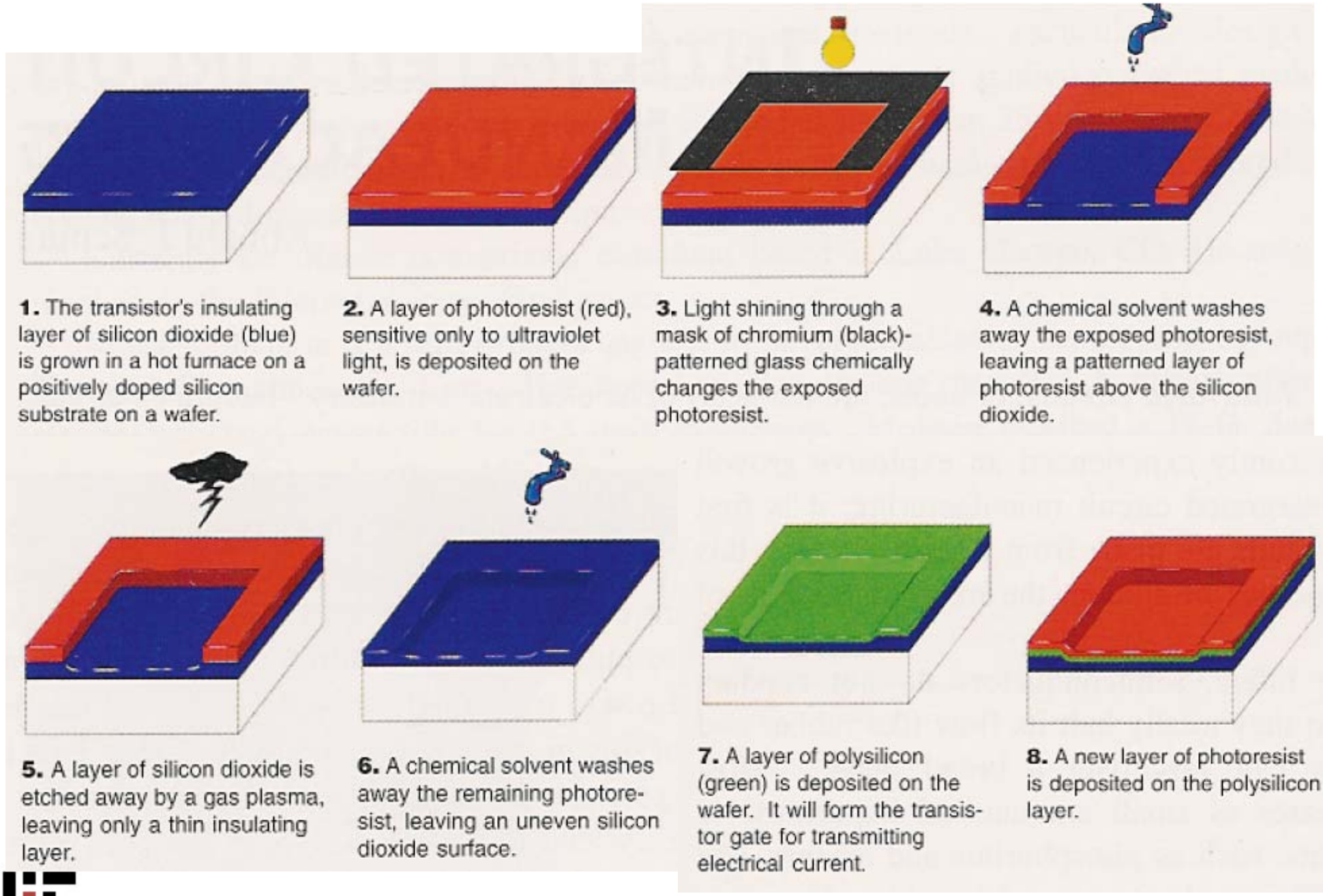
Semiconductor Process Variation

February 7, 2008

Agenda

- The Semiconductor Fabrication Process
  - Manufacturing process control
- Types of Variation in Microfabrication
  - Defects vs. parametric variations
  - Temporal variations: wafer to wafer (run to run)
  - Spatial variations: wafer, chip, and feature level
- Preview of manufacturing control techniques
  - Statistical detection/analysis of variations
  - Characterization/modeling of processes & variation
  - Process optimization & robust design
  - Feedback control of process variation

Semiconductor Fabrication Process, Part 1



1. The transistor's insulating layer of silicon dioxide (blue) is grown in a hot furnace on a positively doped silicon substrate on a wafer.

2. A layer of photoresist (red), sensitive only to ultraviolet light, is deposited on the wafer.

3. Light shining through a mask of chromium (black)-patterned glass chemically changes the exposed photoresist.

4. A chemical solvent washes away the exposed photoresist, leaving a patterned layer of photoresist above the silicon dioxide.

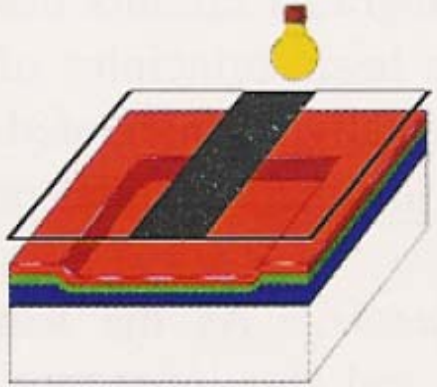
5. A layer of silicon dioxide is etched away by a gas plasma, leaving only a thin insulating layer.

6. A chemical solvent washes away the remaining photoresist, leaving an uneven silicon dioxide surface.

7. A layer of polysilicon (green) is deposited on the wafer. It will form the transistor gate for transmitting electrical current.

8. A new layer of photoresist is deposited on the polysilicon layer.

Semiconductor Fabrication Process, Part 2

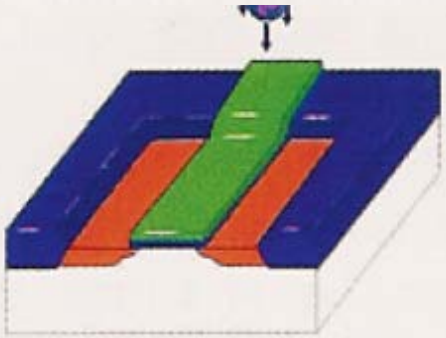


9. Light shining through a new patterned mask chemically changes the photoresist that is exposed to the light.

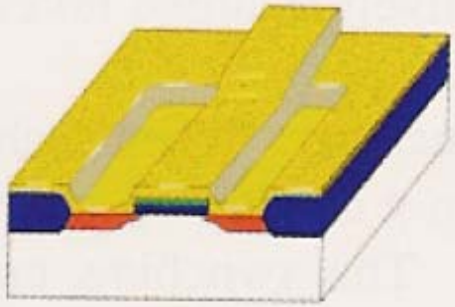
10. A chemical solvent removes the exposed photoresist, leaving a patterned layer of photoresist above the polysilicon.

11. Polysilicon and a thin layer of silicon dioxide are removed by etching, exposing the underlying silicon substrate (white).

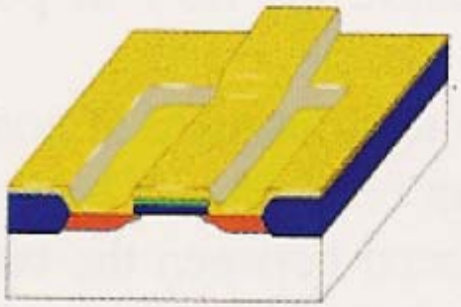
12. A chemical solvent washes away the remaining photoresist, leaving the polysilicon transistor gate structure (green).



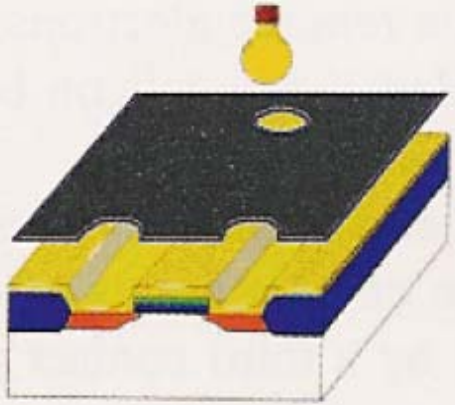
13. Phosphorous atoms are implanted in the positively doped silicon substrate, forming the source and drain as negatively charged wells (orange).



14. A new layer of silicon dioxide is deposited. It will insulate the transistor structure, except for metal contacts that will be added.

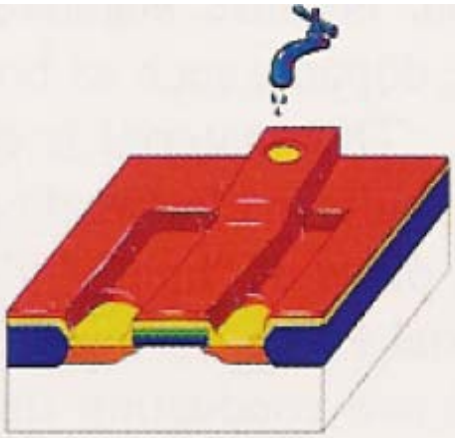


15. A layer of photoresist is deposited on the wafer, in preparation for metal contacts to the source, drain, and gate of the transistor.

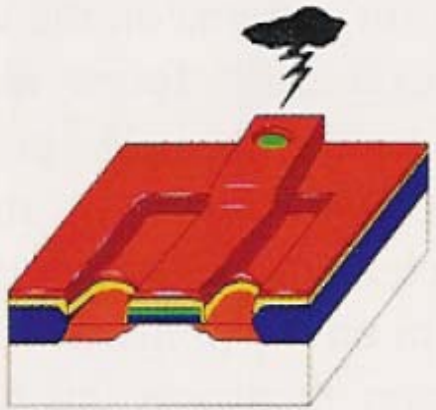


16. Light shining through a patterned mask chemically alters most of the photoresist, except three small areas for metal contacts.

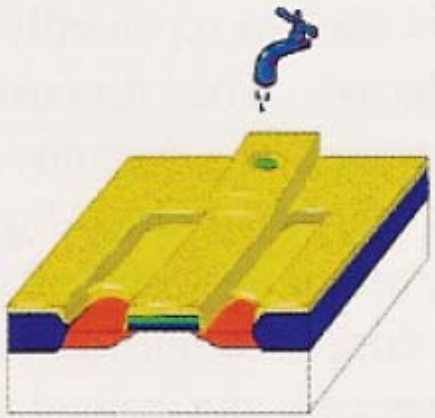
Semiconductor Fabrication Process, Part 3



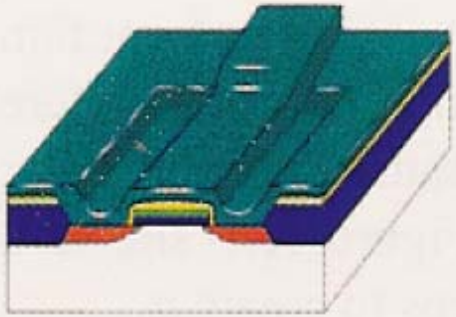
17. A chemical solvent removes the exposed photoresist, opening access to three small areas of silicon dioxide.



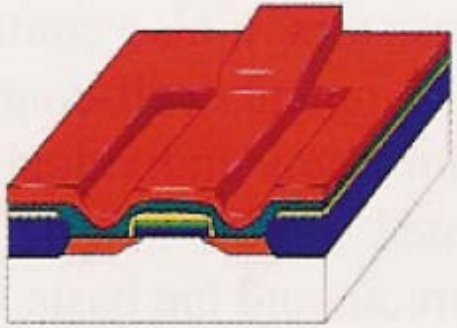
18. Dry etch removes the exposed silicon dioxide, opening shafts to the negatively doped substrate and the polysilicon.



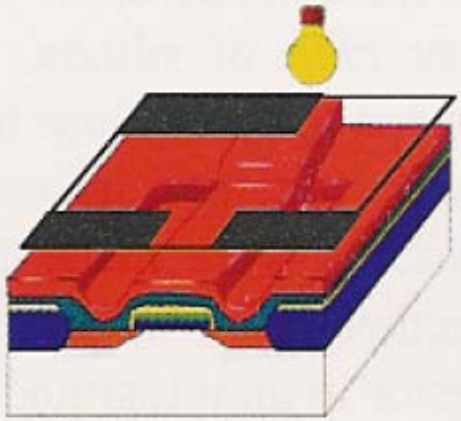
19. A chemical solvent removes the photoresist. The negatively doped source and drain (orange) and the polysilicon gate (green) are opened to metal contacts.



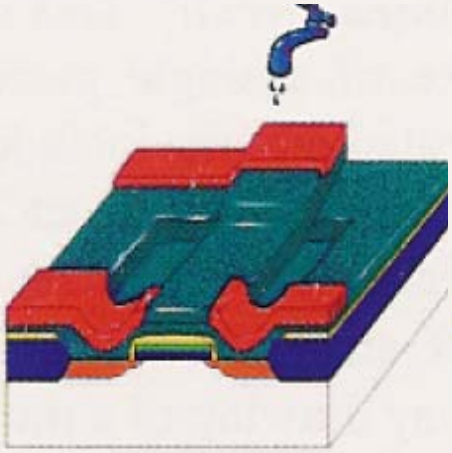
20. Aluminum (blue-green) is deposited over the surface and inside the three shafts. It will provide electrical connections.



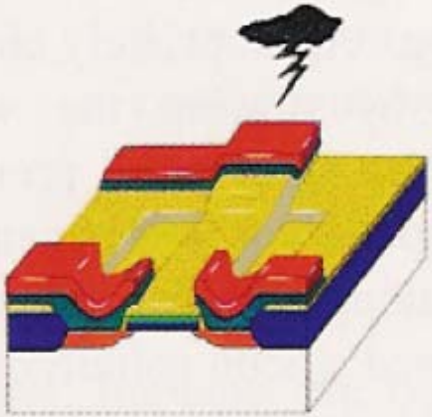
21. A fourth layer of photoresist is deposited on the wafer.



22. Light shining through the fourth patterned mask chemically changes the exposed photoresist.

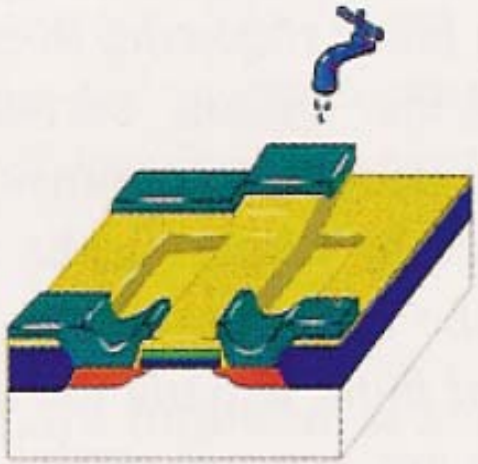


23. A chemical solvent removes the exposed photoresist, creating a photoresist pattern above the aluminum.

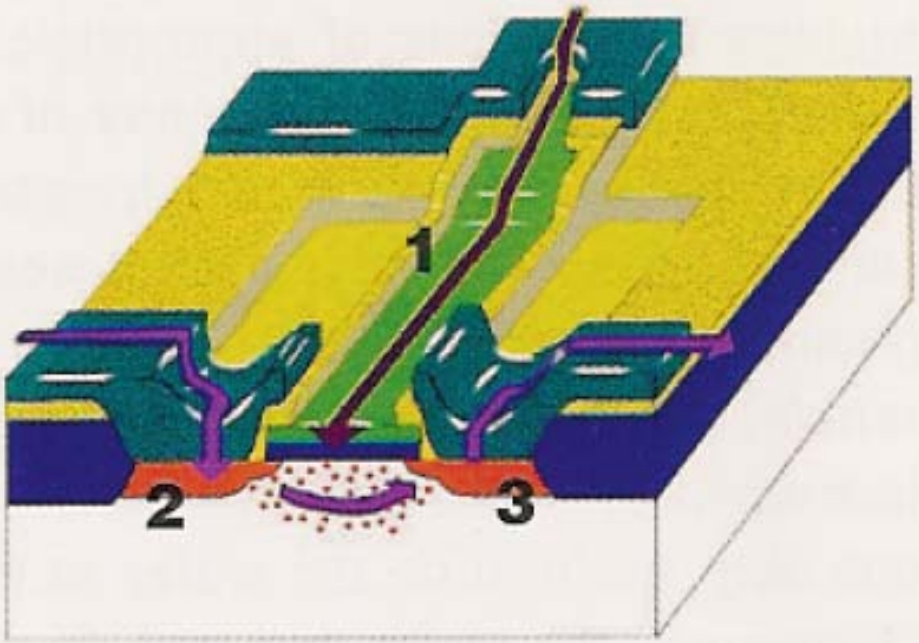


24. The exposed aluminum is etched away, leaving aluminum "wires" that will carry current to and from the transistor.

Semiconductor Fabrication Process, Part 4



25. The photoresist is removed with a chemical solvent, completing the transistor. Many transistors are created simultaneously.



The finished transistor operates as a switch. If no electrical charge is applied to the polysilicon gate (**1**), then no current flows from the negatively charged source (**2**) to the negatively charged drain (**3**). If a positive electrical charge is applied to the gate, it acts through the thin insulating layer of silicon dioxide (blue), creating a channel of negative charge. This channel allows current to flow from source to drain, and on through the aluminum connectors to other parts of the integrated circuit.

(Semiconductor) Manufacturing Process Control

Image removed due to copyright restrictions. Please see Fig. 26 in Boning, D. S., et al. "A General Semiconductor Process Modeling Framework." *IEEE Transactions on Semiconductor Manufacturing* 5 (November 1992): 266-280.

Agenda

- The Semiconductor Fabrication Process
  - Manufacturing process control
- Types of Variation in Microfabrication
  - Defects vs. parametric variations
  - Temporal variations: wafer to wafer (run to run)
  - Spatial variations: wafer, chip, and feature level
- Preview of manufacturing control techniques
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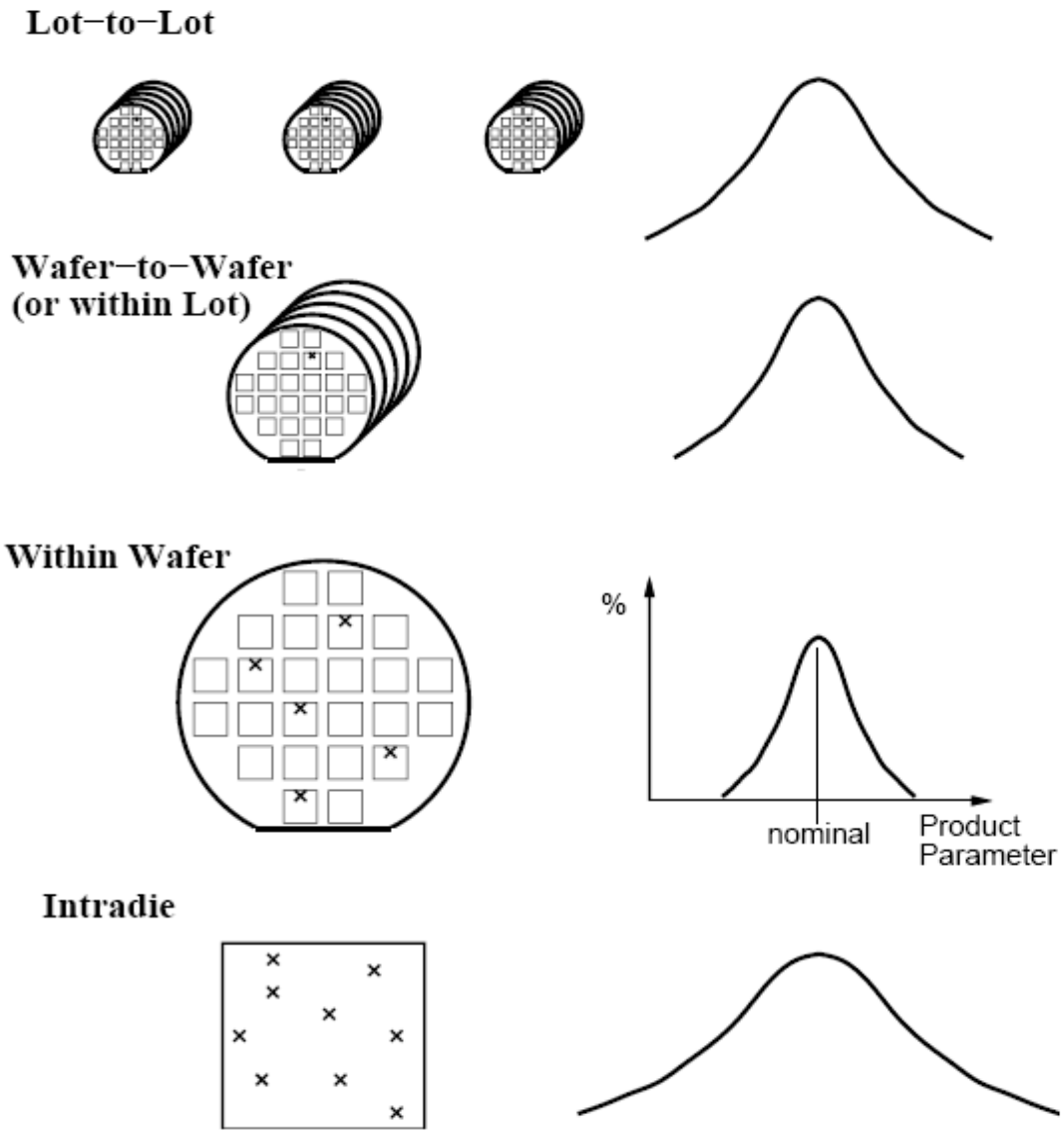
Defect vs. Parametric Variation

Yield & Variation from Defects

- Electrical test
  - measure shorts in test structures for different spacings between patterned lines (at or near the “design rule” or DR feature size)
  - measure opens in other test structures

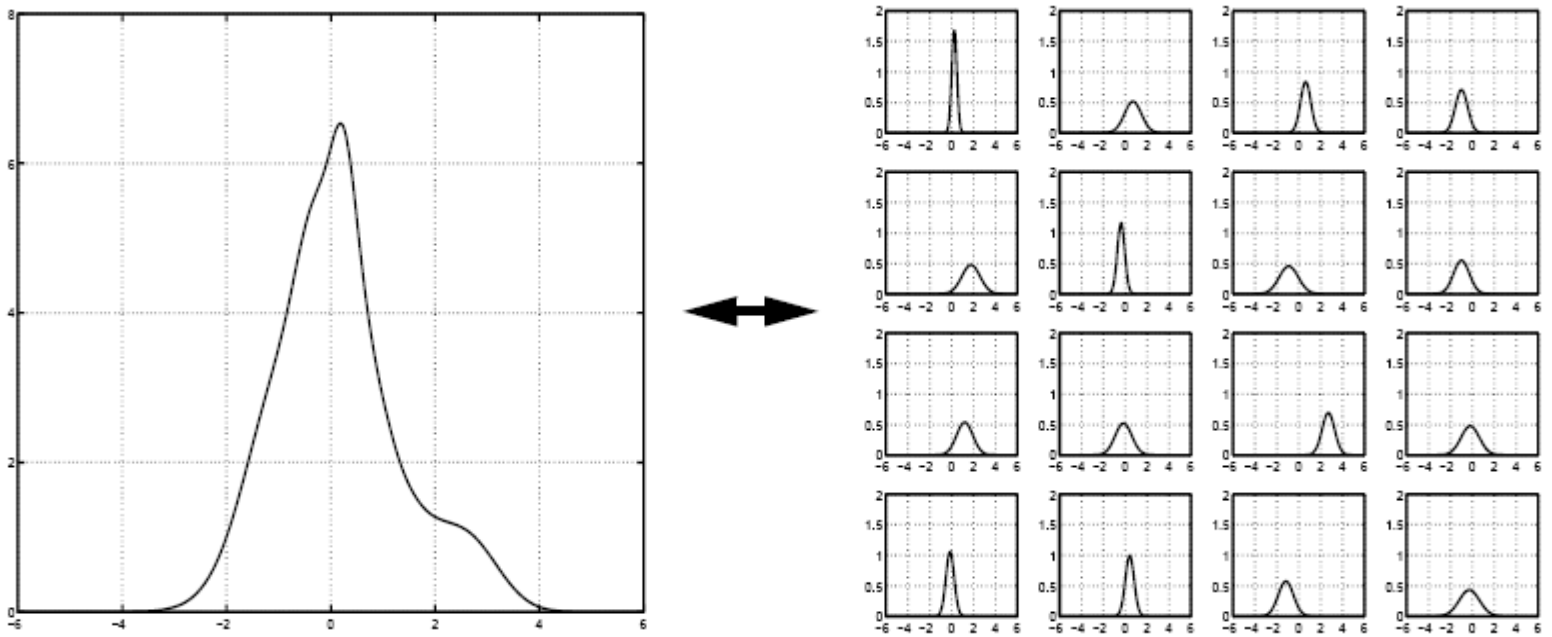
Images removed due to copyright restrictions. Please see: Hess, Christopher. "Test Structures for Circuit Yield Assessment and Modeling." *IEEE International Symposium on Quality Electronics Design*, 2003.

Spatial vs. Temporal Variation



- Temporal Variation
  - Equipment drift lot-to-lot or wafer-to-wafer
  - Typical concern of process control
- Spatial Variation
  - Within-lot (batch tubes)
  - Within-wafer (equipment uniformity)
  - Within-chip: boundary between process control & process integration
- "Signature" at different time or space scale is key lever to separating variation sources

Systematic vs. Random Variation

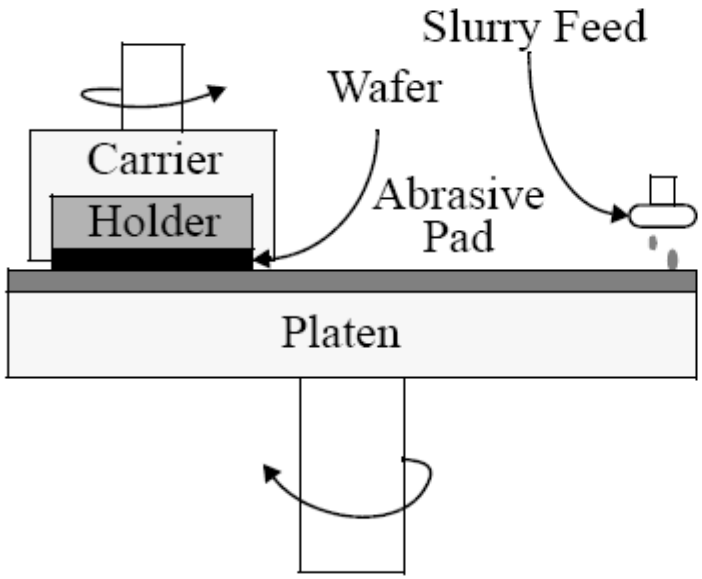


- Multiple systematic effects appear as "random" variance
- Goal: Isolate systematic or deterministic components
- What is repeatable can be dealt with:
  - Focus technology development or variation reduction efforts
  - Process control approaches to minimize
  - Device or circuit design rules to compensate for what remains

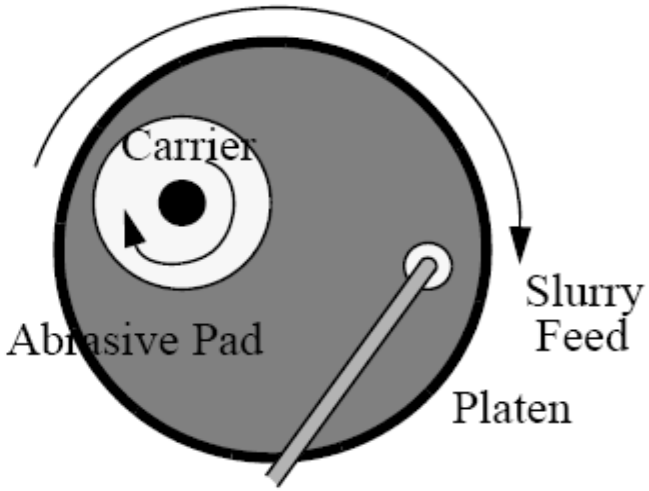
Temporal Variation

Chemical Mechanical Polishing

Side View



Top View

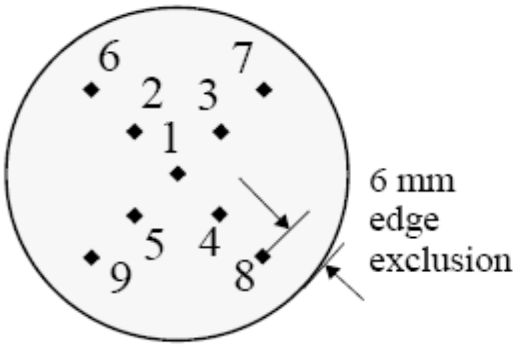


- CMP is critical to advanced IC interconnect technologies
- Key capability: "global" planarization of surface topography
- Active research in process, equipment, and sensor development

CMP Limitations and Control Challenges

- Limited understanding of the process
- Substantial drifts in equipment operation
- Lack of in-situ sensors

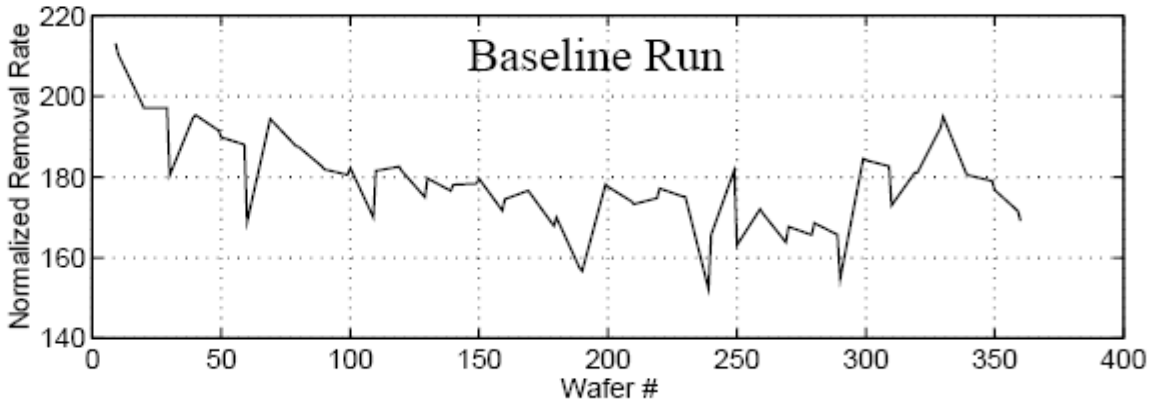
Blanket oxide wafer:

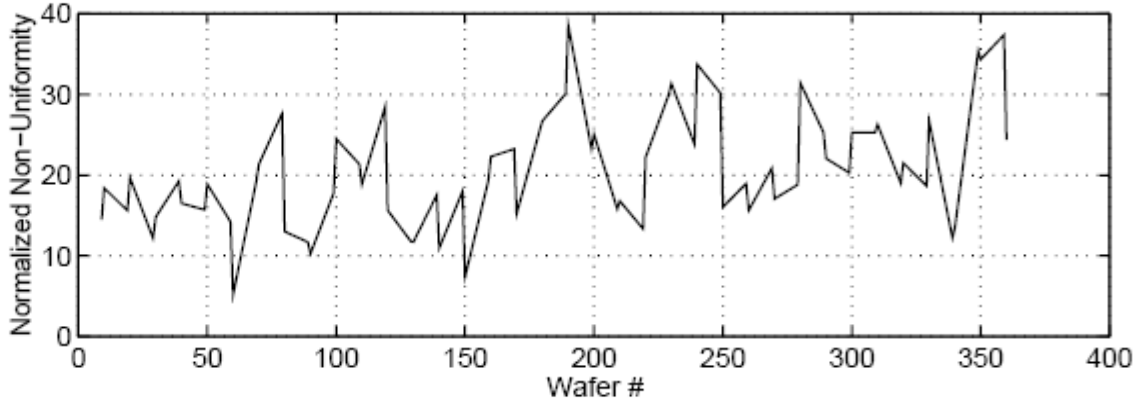


Targets:

Removal Rate

Nonuniformity

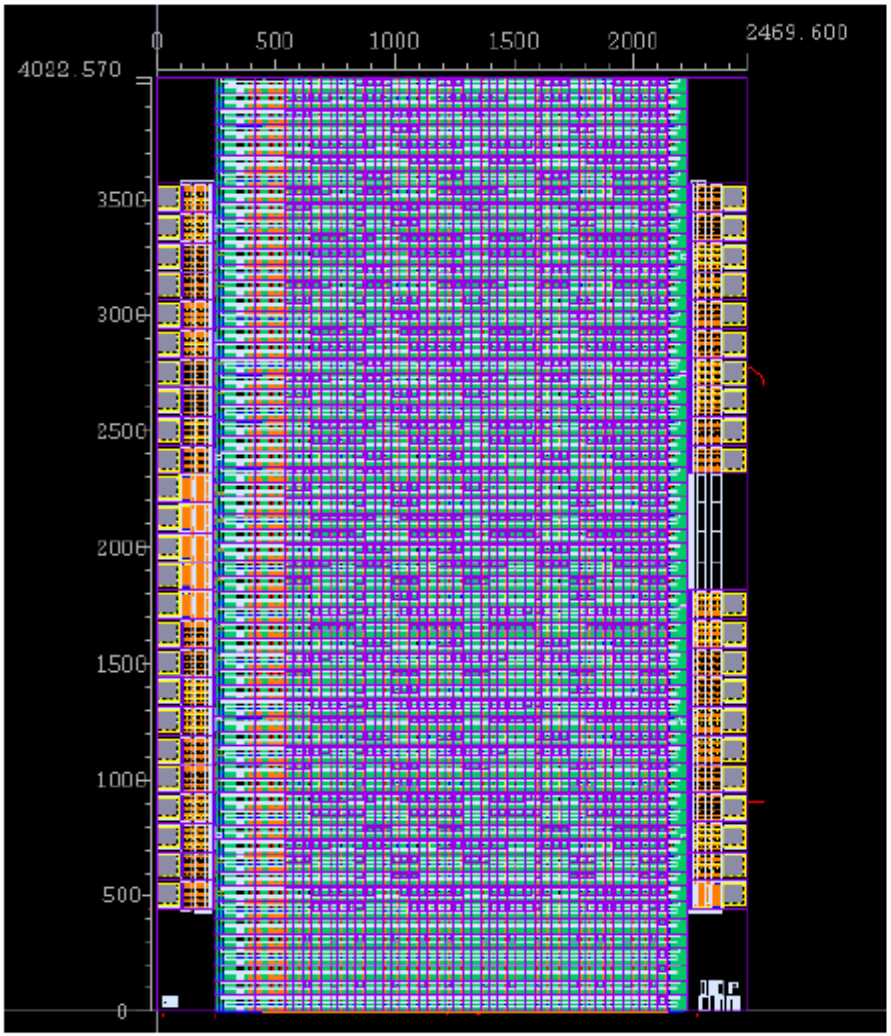




Spatial Variation

- Wafer scale
- Chip scale
- Feature scale

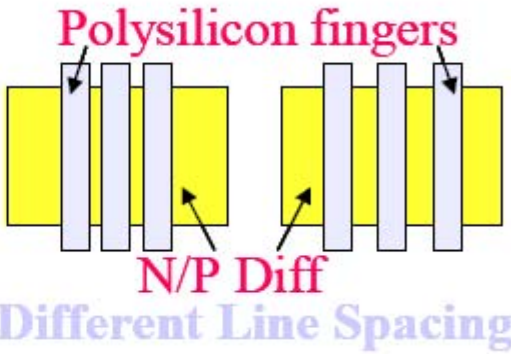
Impact of Spatial Variation on Integrated Circuit Performance

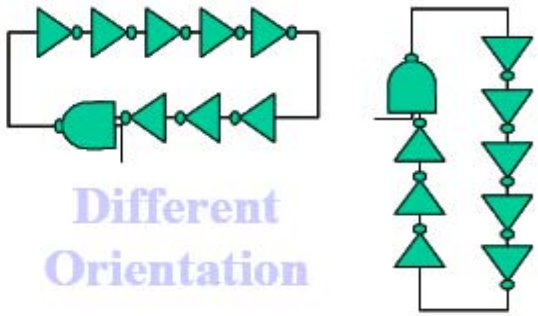


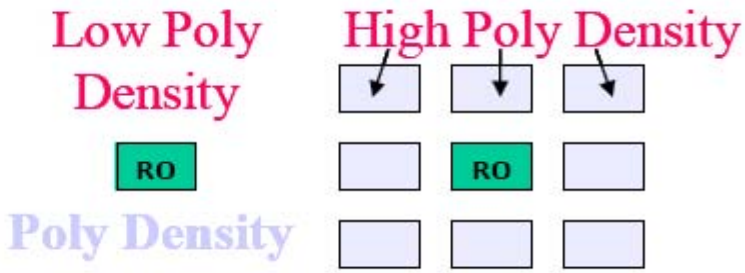
- Ring oscillator (RO) as "stand-in" for circuit speed
- Heavily replicated RO test structures across chip
  - 60 rows
  - 43 tiles/row (1 RO/tile)
  - 2580 total tiles
- 2.4 mm x 4.0 mm die size
- Fabricated in 0.25 um TSMC technology
  - 35 packaged chips from same wafer

Ring Oscillator Test Structures

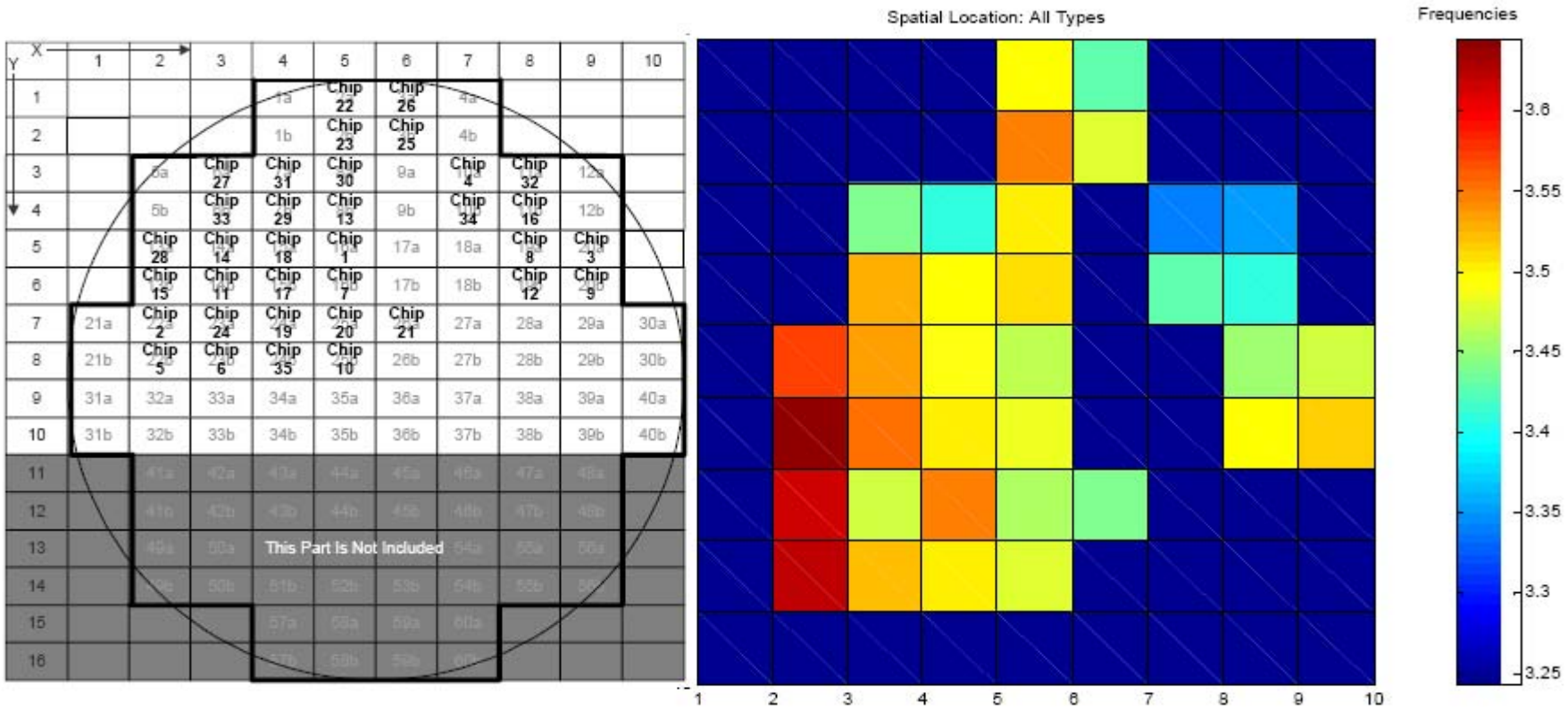
- Each tile: device variation structures consisting of ring oscillators with only inverters (no additional load)
- Key layout variations studied:
  - proximity effect -- RO finger spacing
  - number of fingers
  - vertical/horizontal orientation
  - etch loading -- local polysilicon pattern density





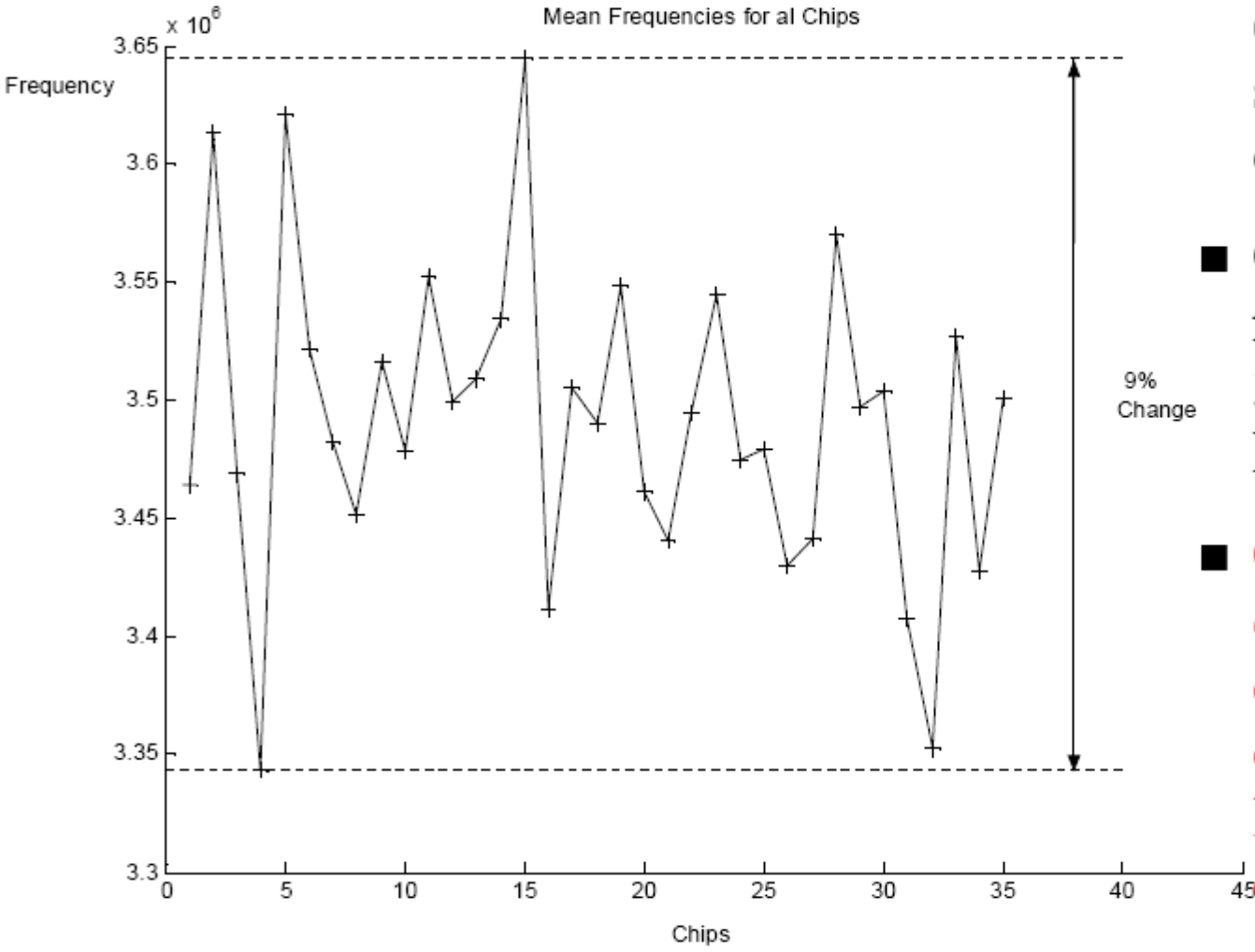


Wafer Scale Variation in RO Speed



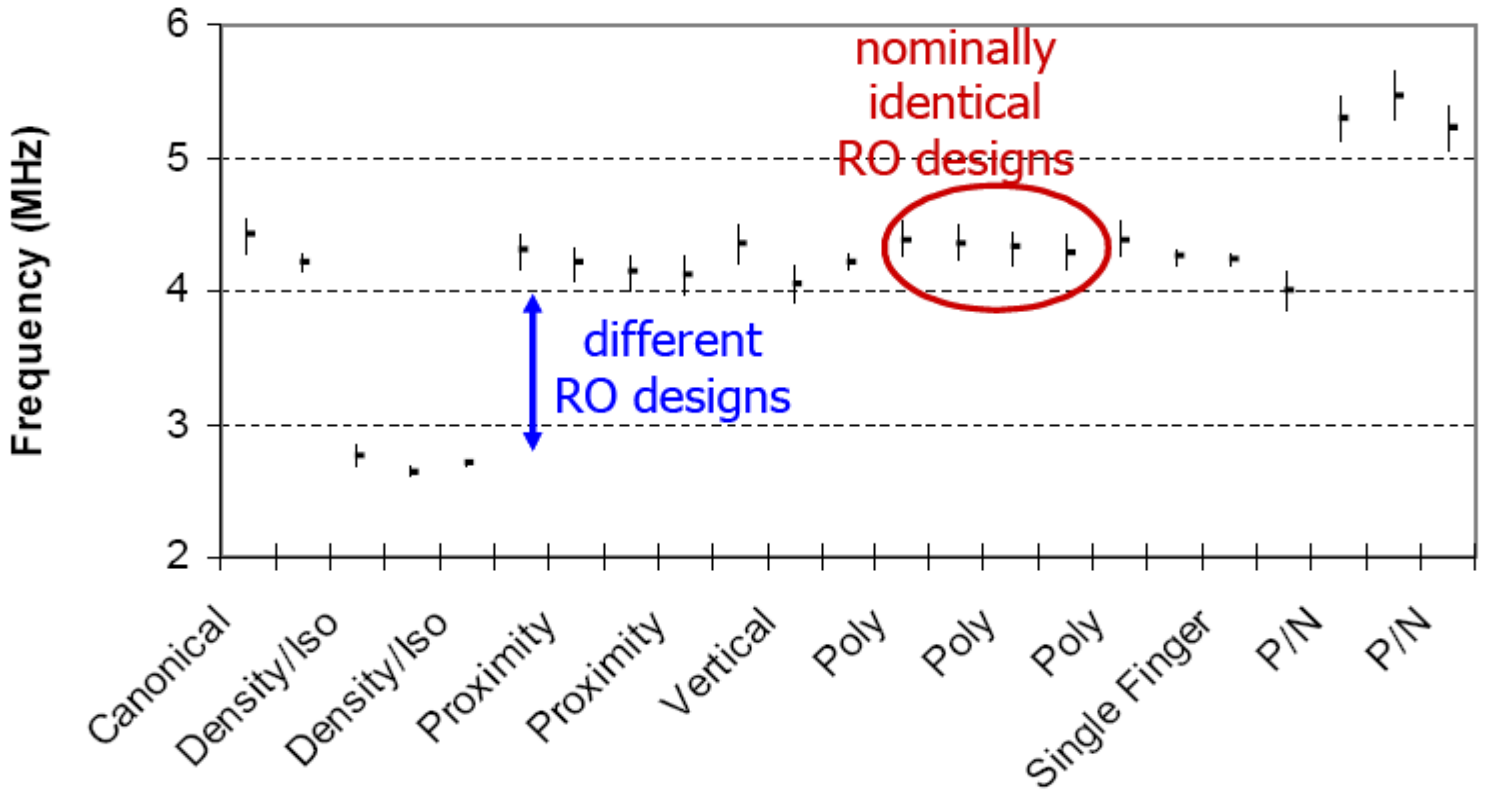
- Chip location on wafer obtained from foundry
- Display chip average frequency at each location
  - Observe clear wafer scale trend
  - Across wafer variation ~9%

Chip to Chip Variation in RO Speed



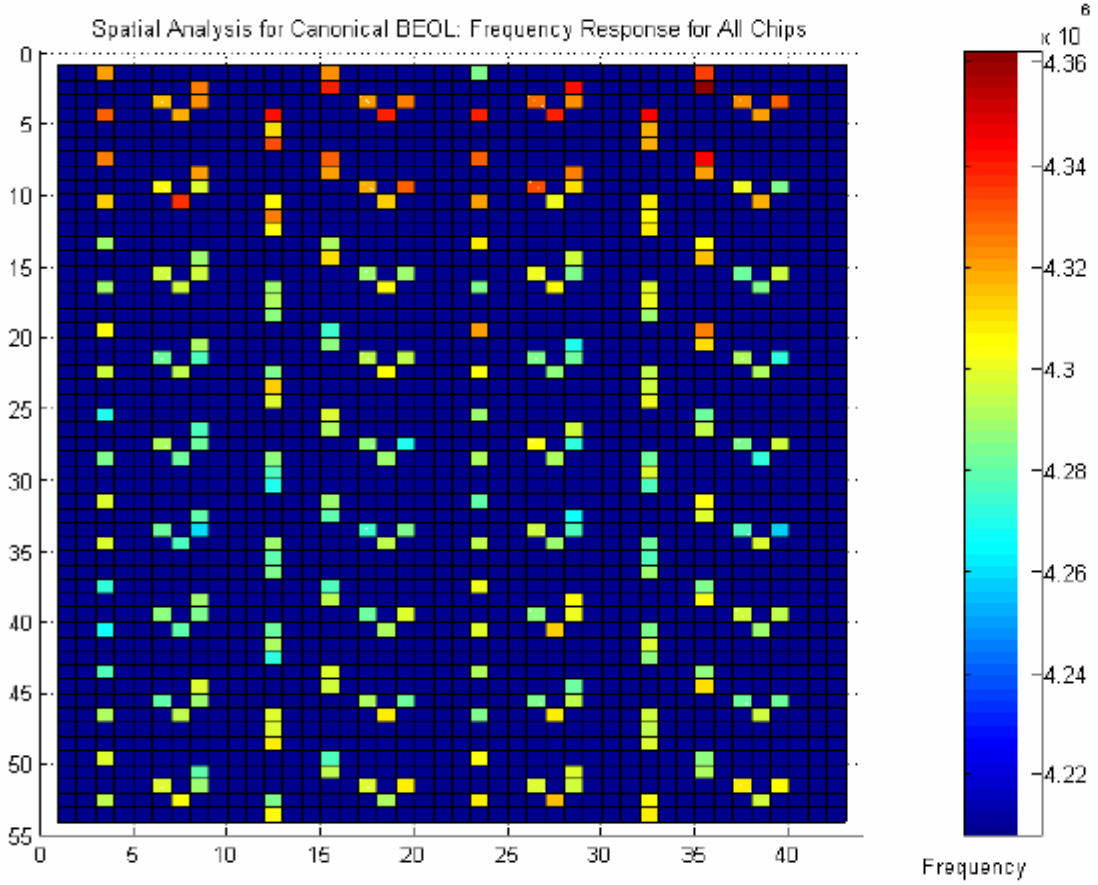
- Chip Mean (average of all structures on each chip)
- Chip to chip range 0.3 MHz: 3.35 to 3.65 MHz, or ~9%
- Question: how does chip to chip effect compare to layout or within chip variation?

Layout Dependent Variation in RO Speed



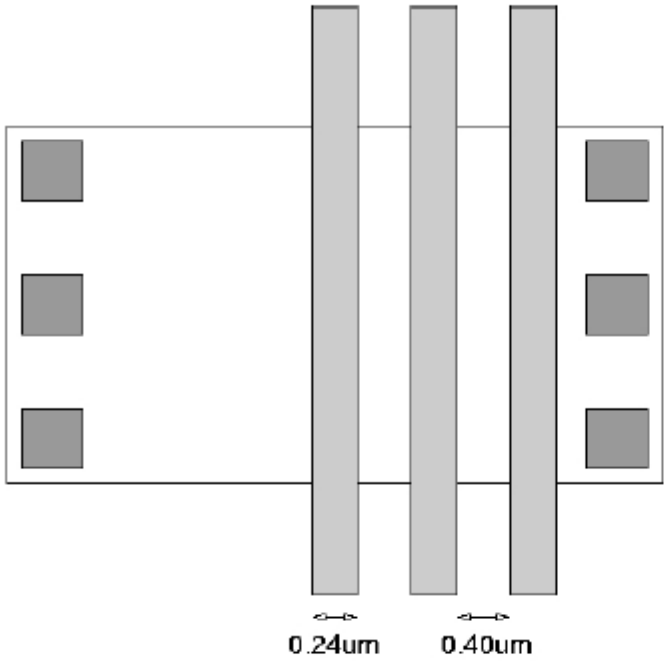
- Plot mean & $1\sigma_f$ frequency for each structure type
- Observation: Layout effect can be huge (10-25%)
- Question: how compare to within chip (replicate) variation?

Within Chip Spatial Trend in RO Speed

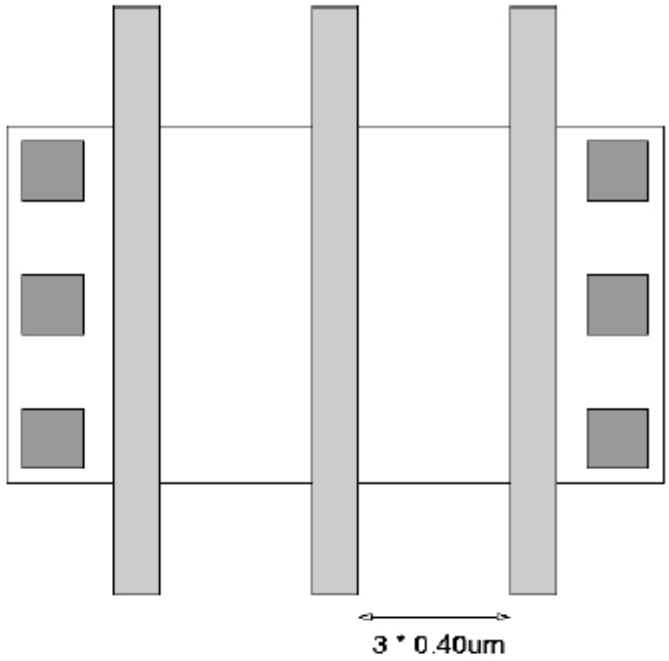


- Map one RO type
  - average across all chips plotted
  - Canoical BEOL RO
- Top to bottom trend
- Total variation:
  - 4.2 MHz to 4.4 MHz (~4%)
- Observation: within chip effect also much less than layout effect

Layout Effect: Poly Proximity



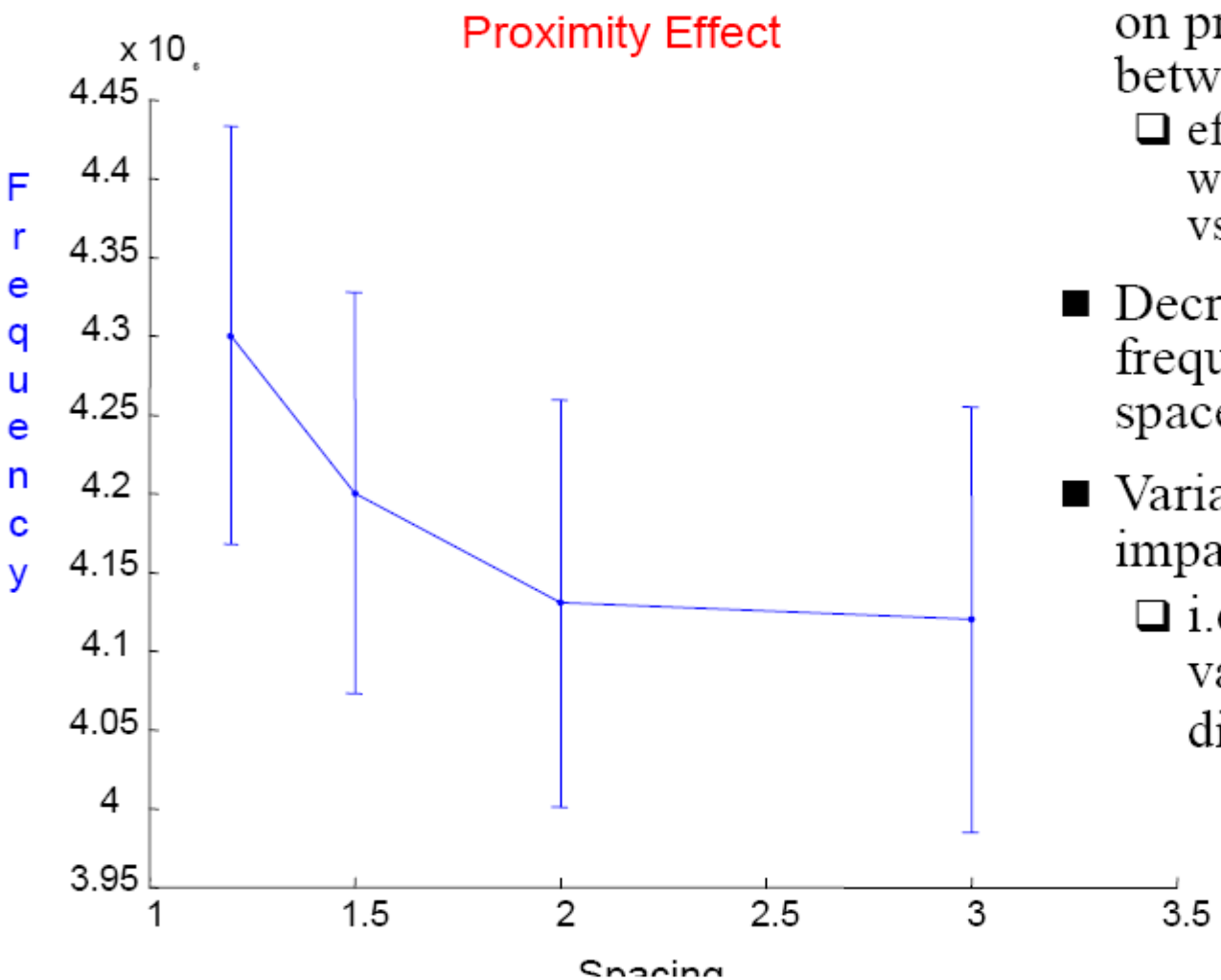
Canonical RO (1X Line–Spacing)



RO3 (3X Line–Spacing)

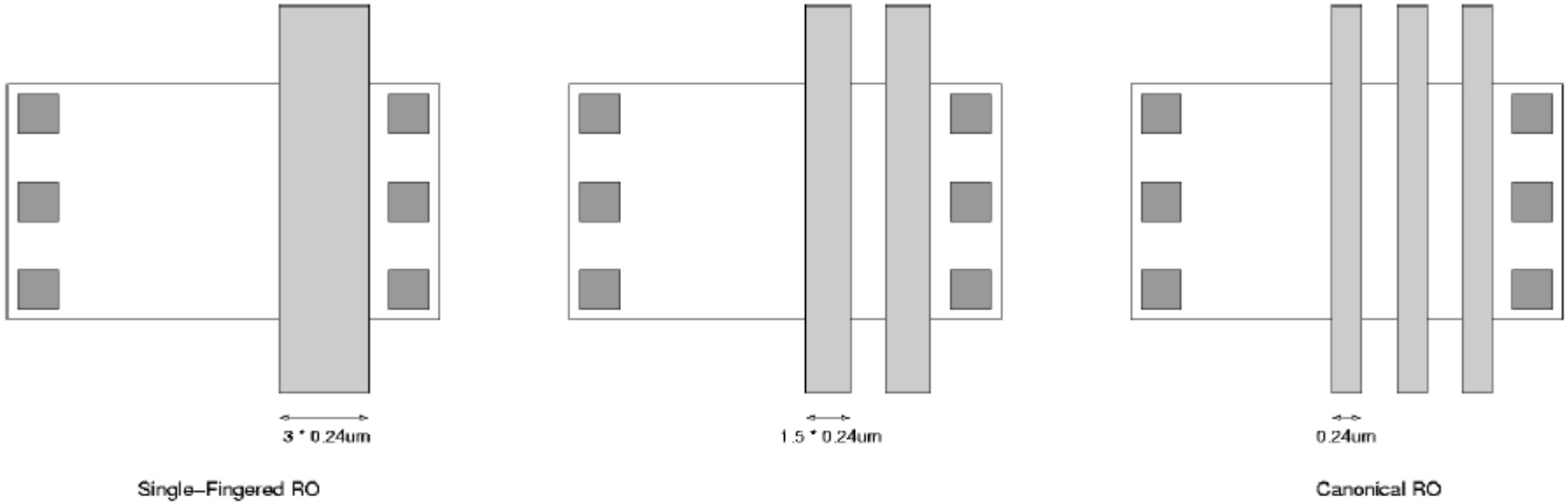
- Three finger P/N devices
- Minimum finger size (0.24 μm)
- 1.2X, 1.5X, 2X, and 3X minimum line spacing (0.40 μm)

Layout Effect: Poly Proximity Results



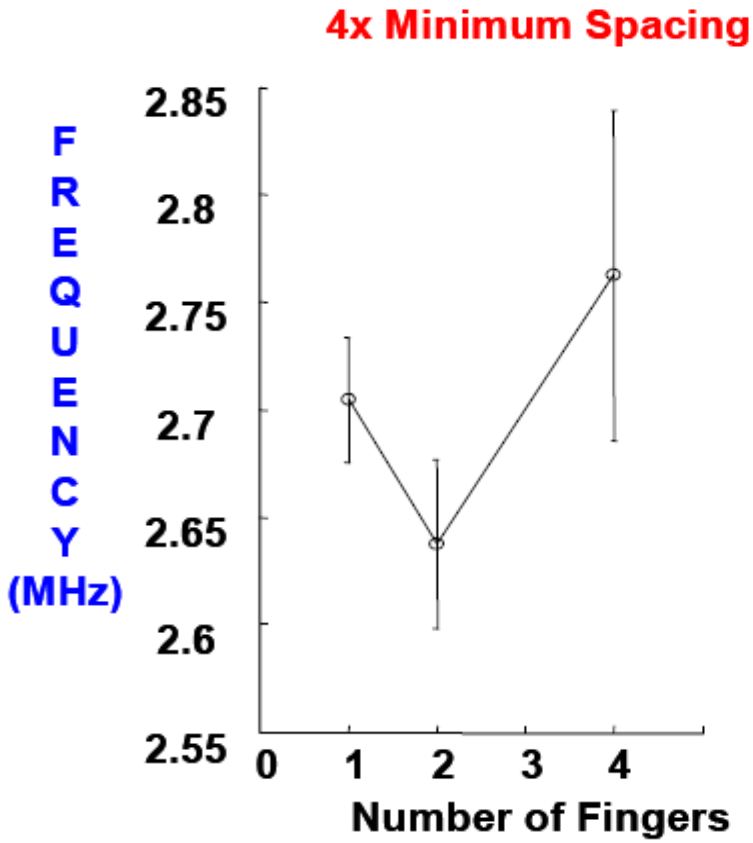
- Clear layout effect based on proximity or spacing between fingers
  - effect comparable to wafer level variation (0.2 vs 0.3 MHz)
- Decreasing mean frequency as the gate space increases
- Variance not srongly impacted by spacing
  - i.e. within chip variation same for different RO spacing

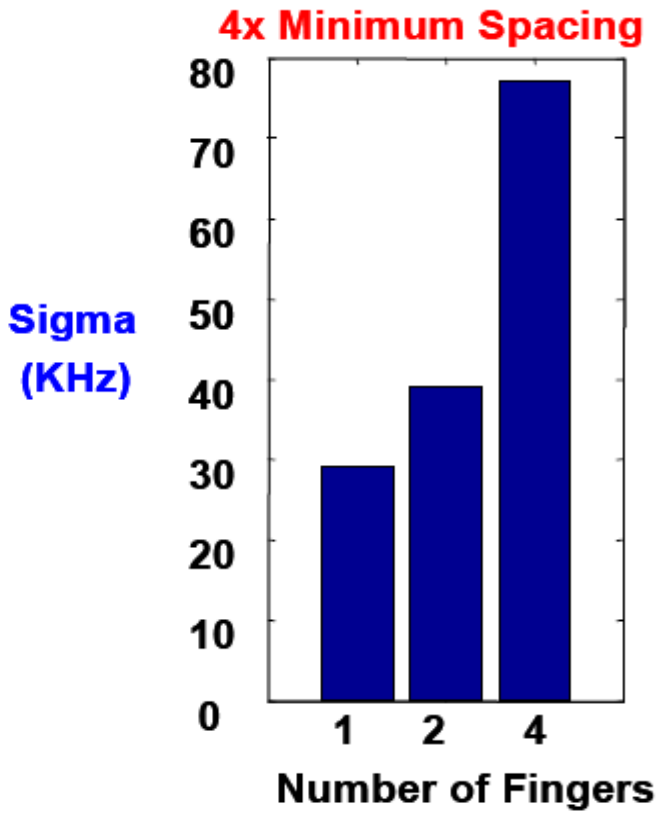
Layout Effect: Finger Spacing



- Total transistor channel length L = 0.72 um
- Allocate gate length across 1, 2, or 3 fingers
- Expect single-fingered RO to be most robust to gate length variation

Layout Effect: Finger Spacing Results





- Average RO frequency is affected by # of fingers
- Variance proportional to # of fingers

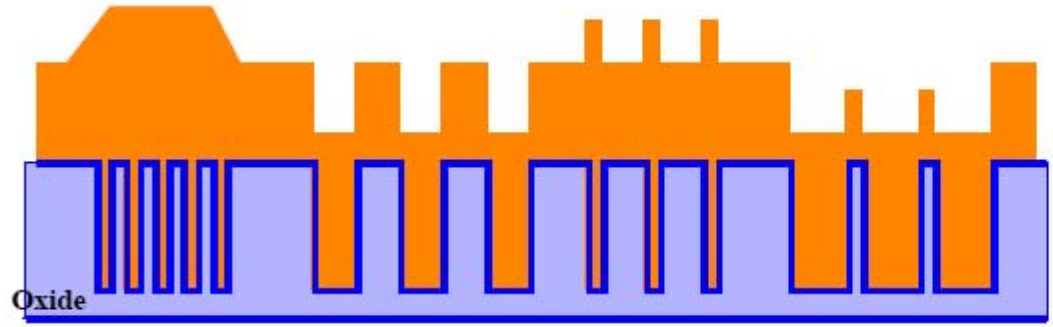
Observations on the Impact of Spatial Uniformity on IC Performance

- Multiple types and sources of spatial variation at work
  - **Wafer level**
  - **Chip level** interactions/trends or neighborhood effects
  - **Feature level** or layout practice effects
  - Each of these can be **large** and important
- Attention needed to specific process sources of variation
- Modeling and control to understand and minimize

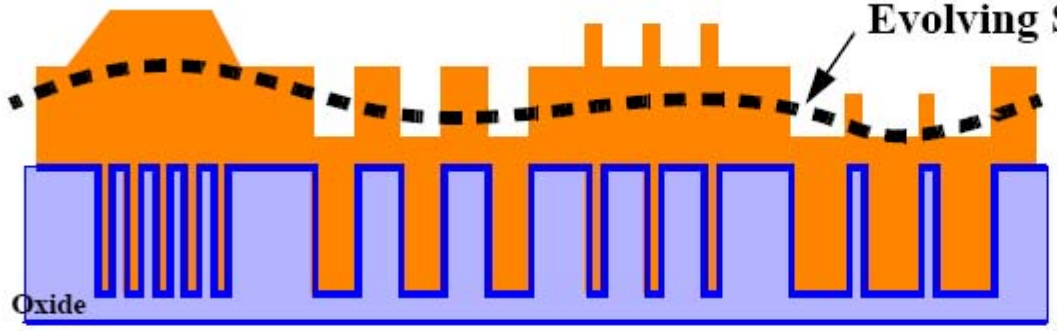
Modeling of Processes and Variation

- Empirical modeling
- Physical modeling

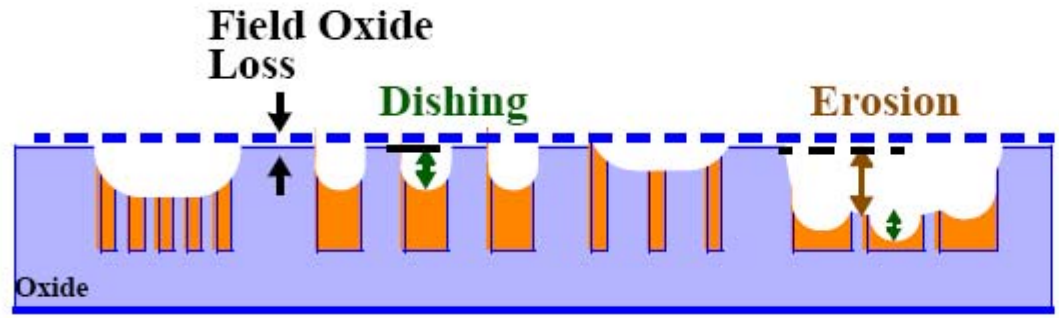
Chip-Scale and Feature-Scale Variation in Copper Electroplating and CMP



Copper Electroplating



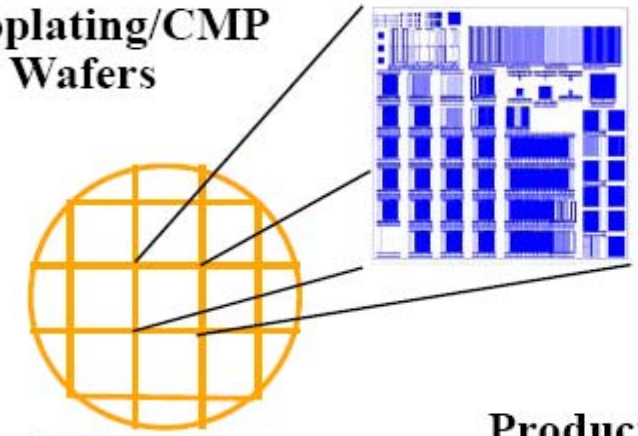
CMP



CMP Overpolish

Electroplating/CMP Characterization Methodology

Electroplating/CMP Test Wafers



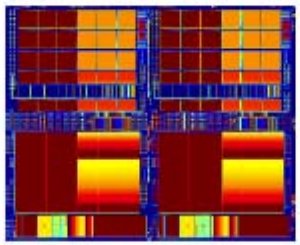
- Plating: Measure step height, array bulge/recess and field copper thickness
- CMP: Measure dishing, erosion and field copper thickness

Model Parameter Extraction

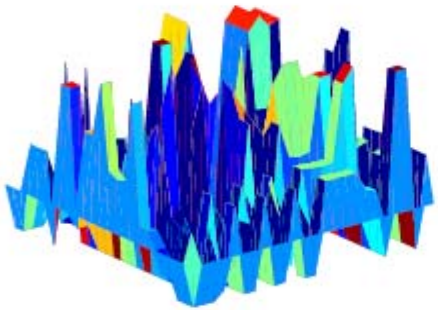
Calibrated ECD Pattern Dependent Model

Calibrated Copper Pattern Dependent Model

Product Chip Layout



Chip-Level Simulation



- Plating: prediction of step height, array height, copper thickness and local pattern density
- CMP: prediction of clearing time, dishing and erosion, final copper line thicknesses

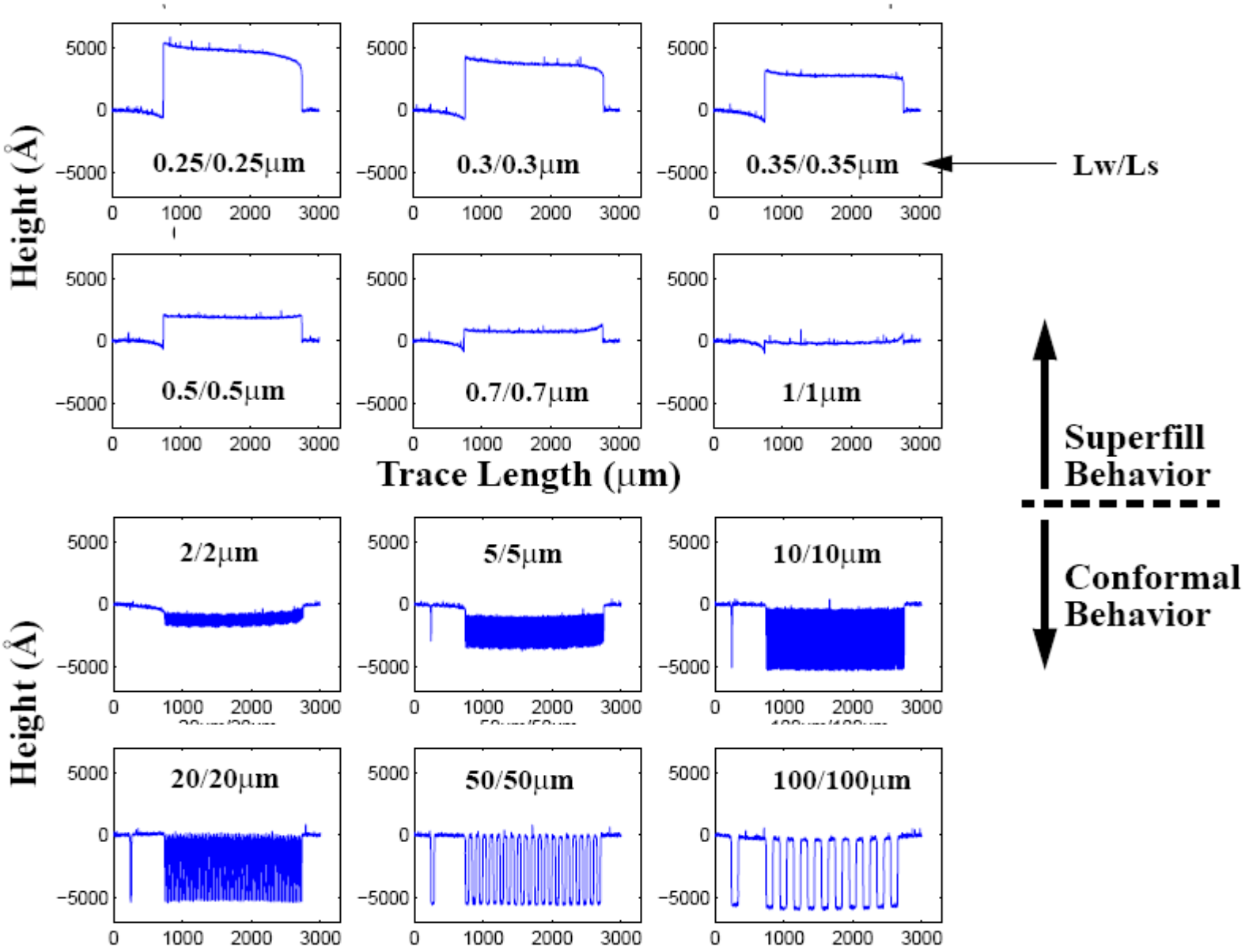
Electroplating Process

- Fixed plating recipe

CMP Process

- Fixed pad, slurry, process settings (pressure, speed, etc)
- Variable polish times

Electroplated Profile Trends: Pitch Structures



Semi-Empirical Model for Feature-Size Dependent Topography Variation

- Physically Motivated Model Variables:
  - Width, Space, 1/Width, and Width*Space
- Semi-Empirical Model Development
  - Capture both conformal regime and superfill regime in one model frame
  - $1/W^2$ and W^2 terms explored as well
- Model Form
  - Array Height (AH):

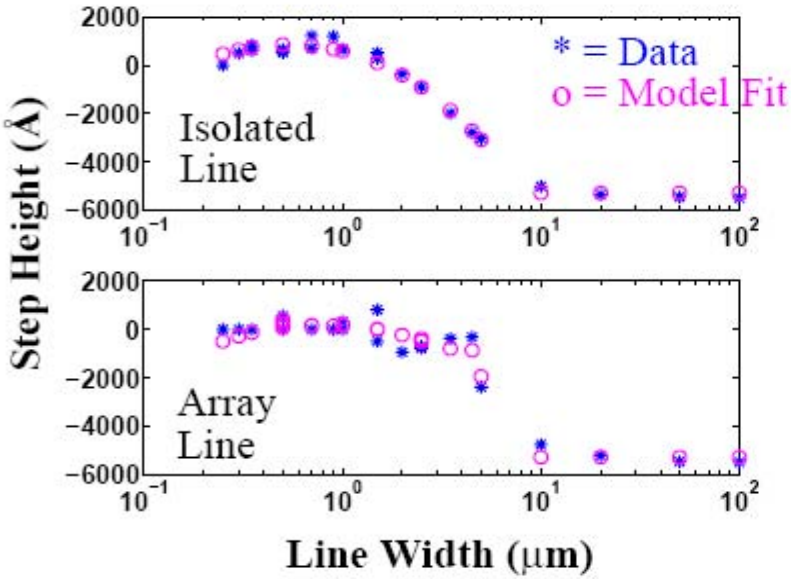
$$AH = a_E W + b_E W^{-1} + c_E W^{-2} + d_E S + e_E W \times S + Const_E$$

  - Step Height (SH):

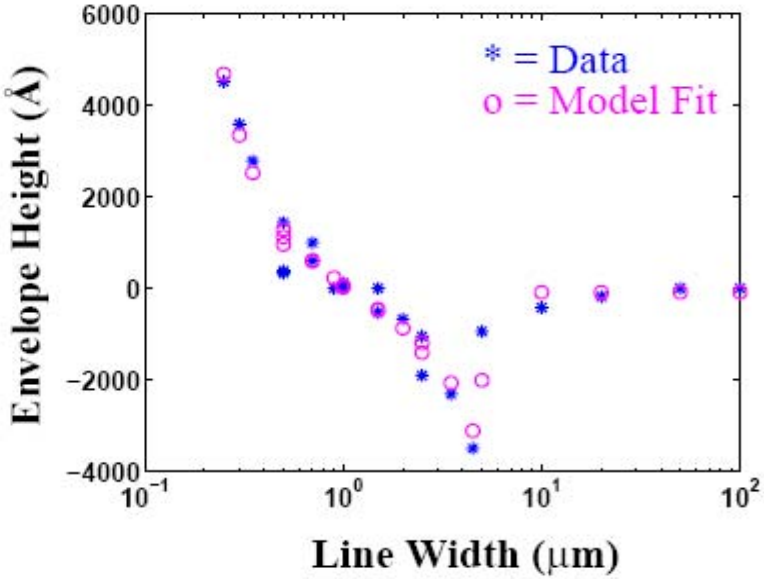
$$SH = a_S W + b_S W^{-1} + c_S W^{2} + d_S S + e_S W \times S + Const_S$$

Model Fit: Step Height and Array Height

Step Height vs. Line Width



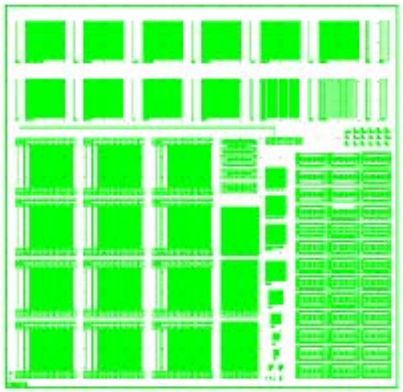
Array Height vs. Line Width

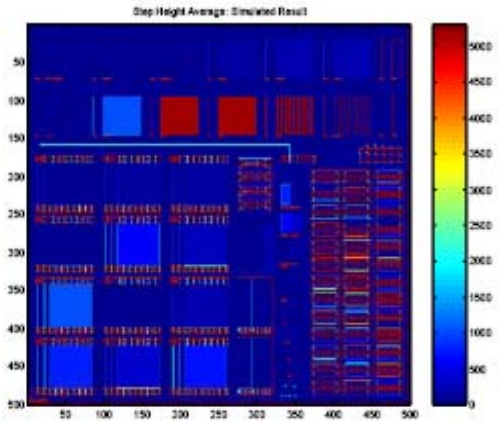


- The models capture both trends well
  - Step Height RMS error = 327 Å
  - Array Height RMS error = 424 Å
- Model coefficients are calibrated and used for chip-scale simulations

Chip-Scale Plating Simulation Calibration

Test Mask

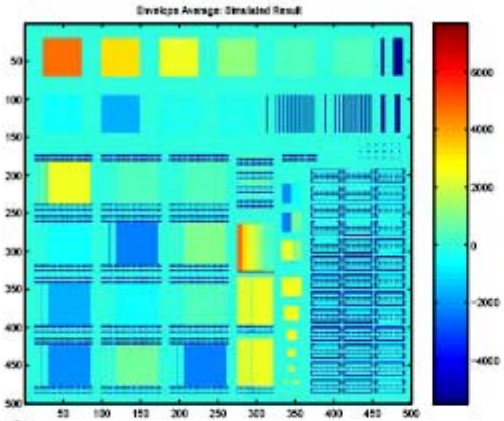




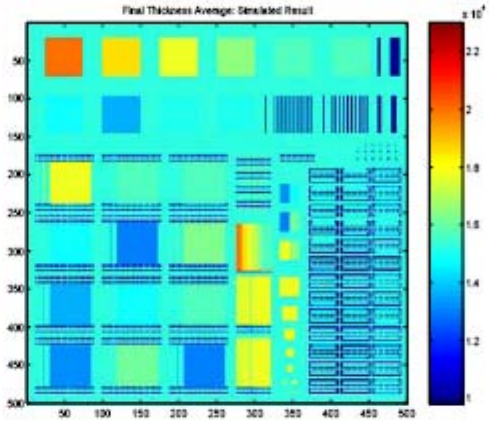
Step Height

RMS Error=420Å

Array Height



RMS Error=440Å

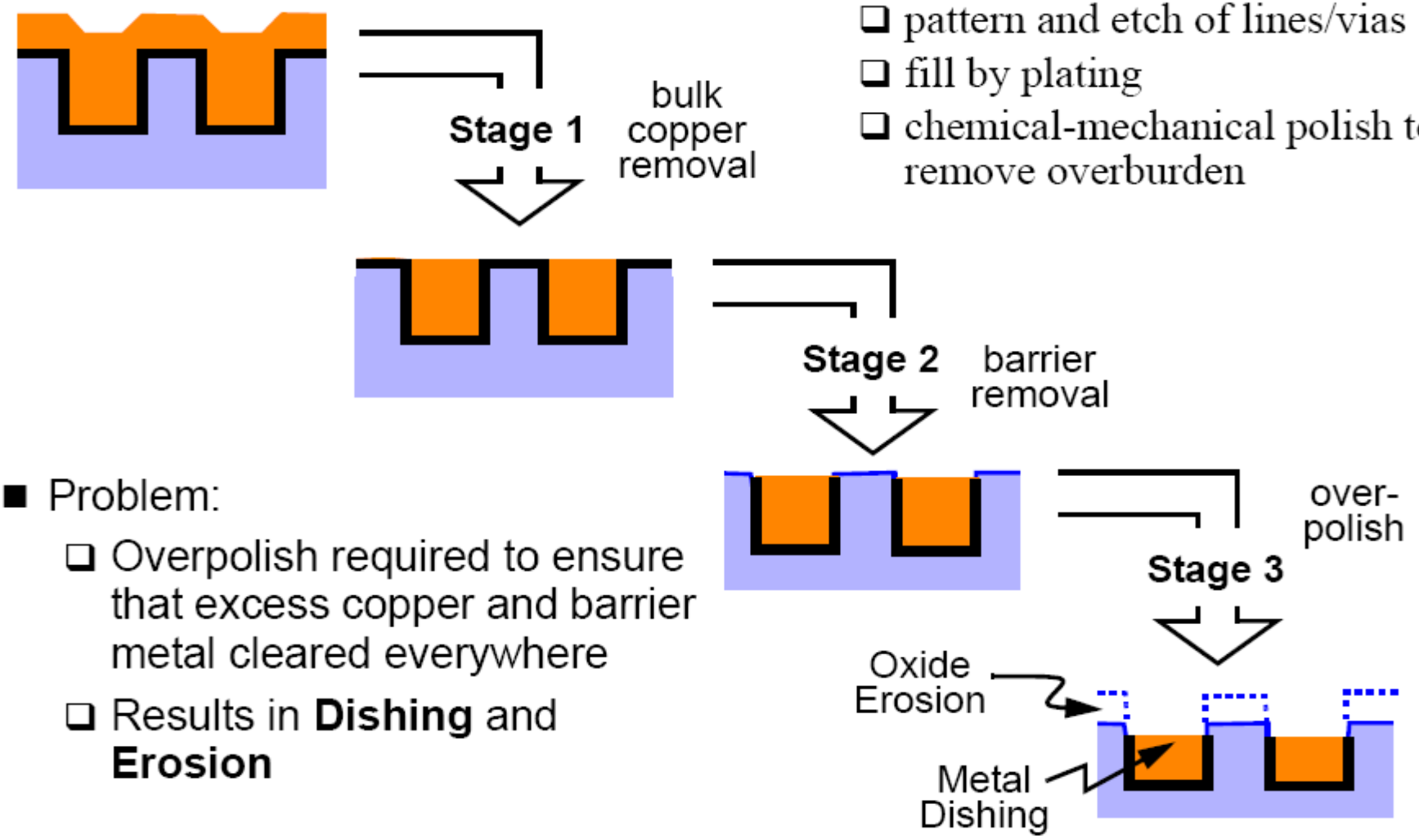


Final Thickness

- Simulated over the entire test mask used to calibrate the model
- RMS errors are slightly greater (about 90Å and 10Å more) than fitting RMS errors since distribution values are used

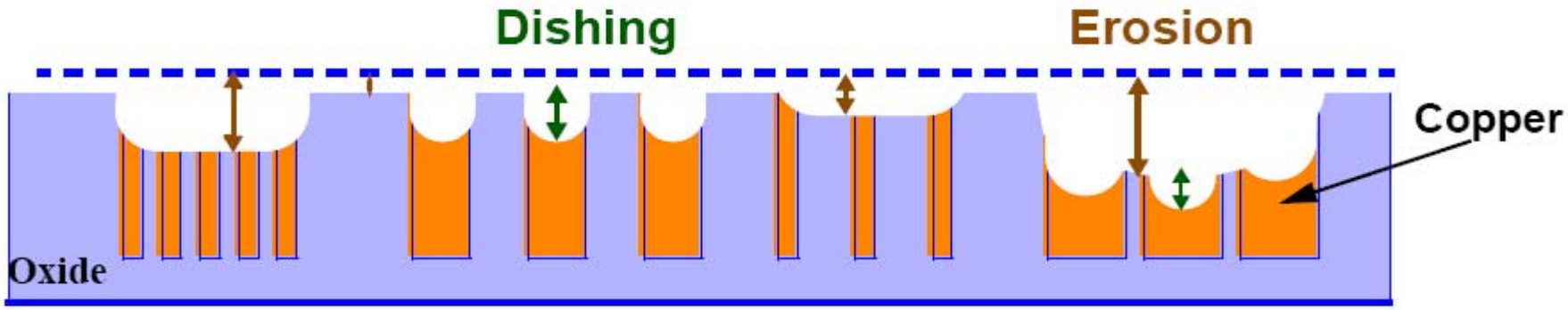
Chip-Scale Variation in Copper CMP

- Copper interconnect formed by
  - pattern and etch of lines/vias
  - fill by plating
  - chemical-mechanical polish to remove overburden

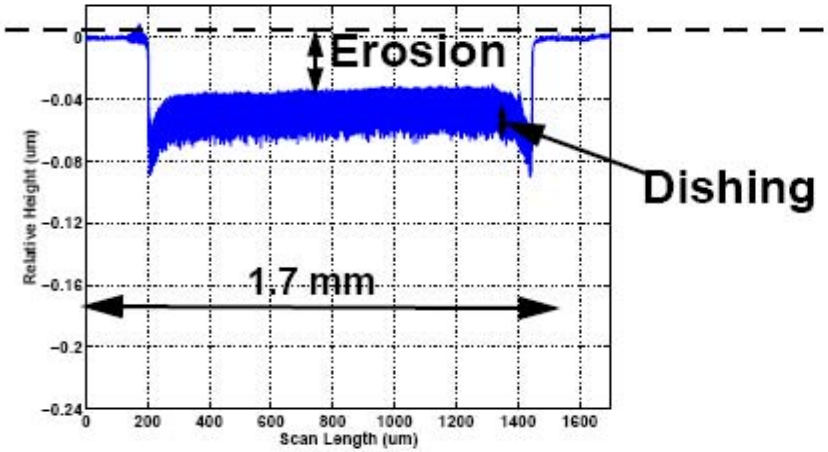


- Problem:
  - Overpolish required to ensure that excess copper and barrier metal cleared everywhere
  - Results in **Dishing** and **Erosion**

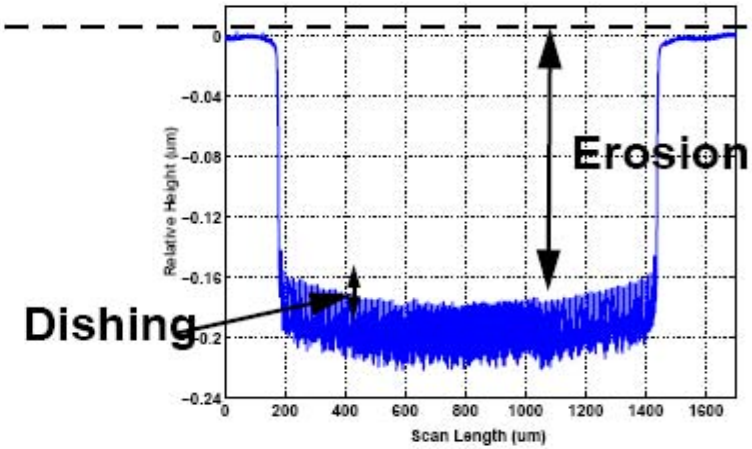
Chip-Scale Variation in Copper CMP



Sample Profilometer Scans



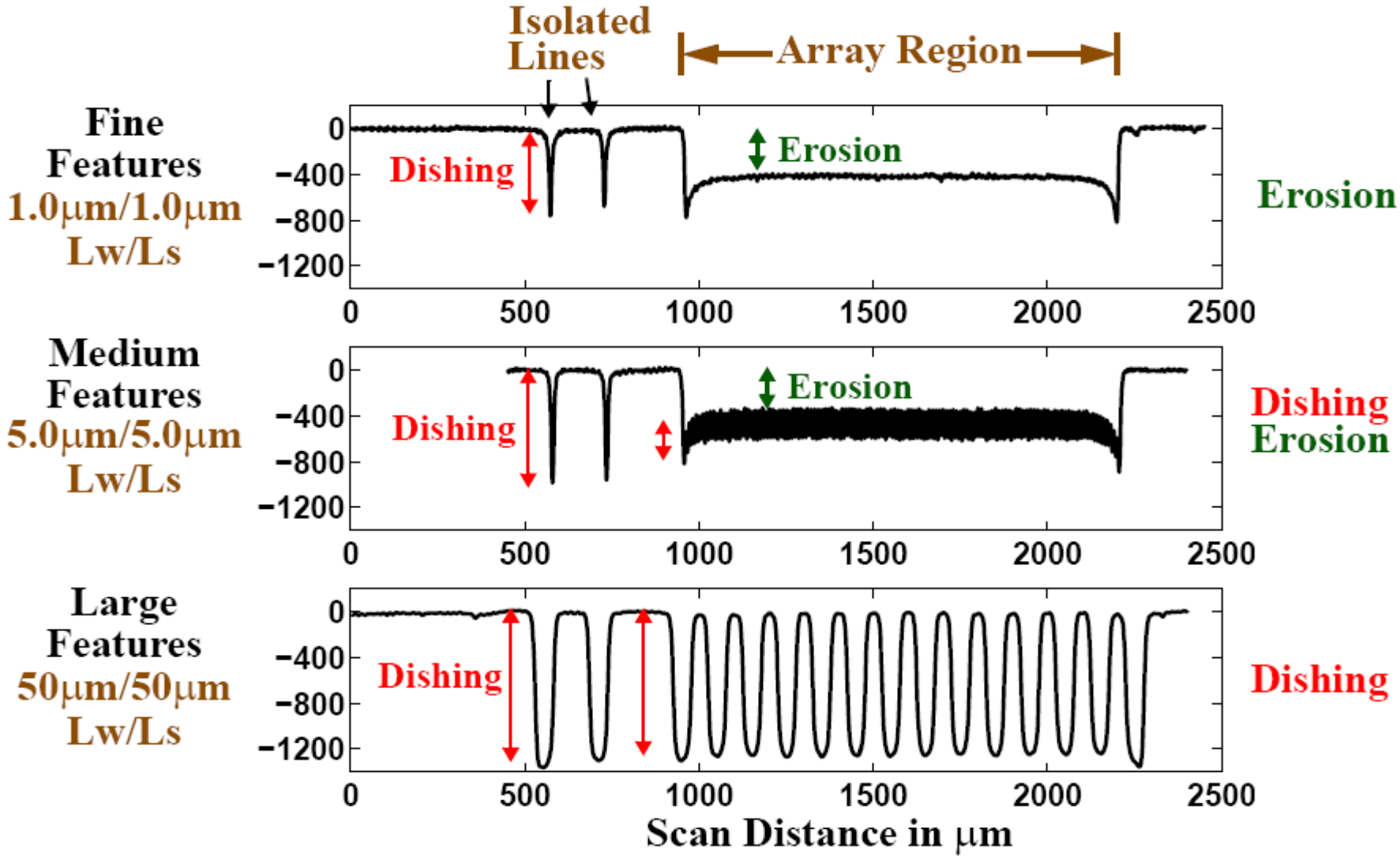
Line width = 1 μm
Line space = 1 μm



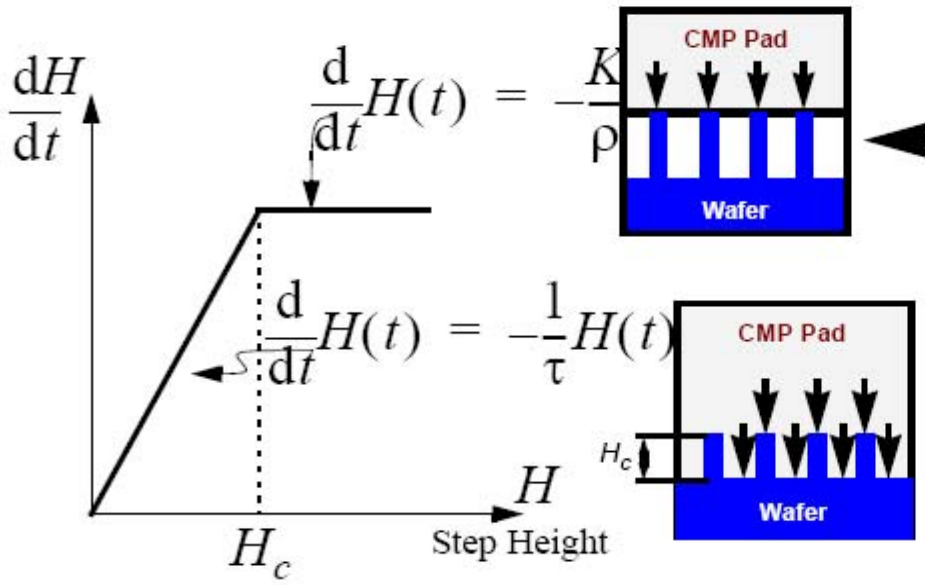
Line width = 9 μm
Line space = 1 μm

Single Layer Surface Profiles and Trends

Surface Profiles (in Å)



Chip-Scale Pattern Density / Step-Height Model

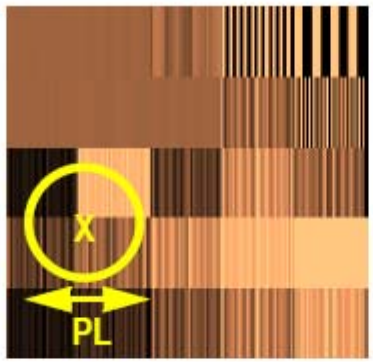


- For large step heights:
  - step height reduction goes as 1/pattern-density

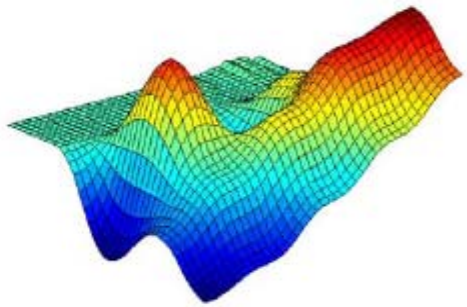
- For small step heights (less than the "contact height"):
  - height reduction proportional to height
  - height decays with time constant τ:

$$H(t) = H_0 e^{-t/\tau}$$

- Calculate *effective density* by averaging local pattern densities over some window/ weighting function

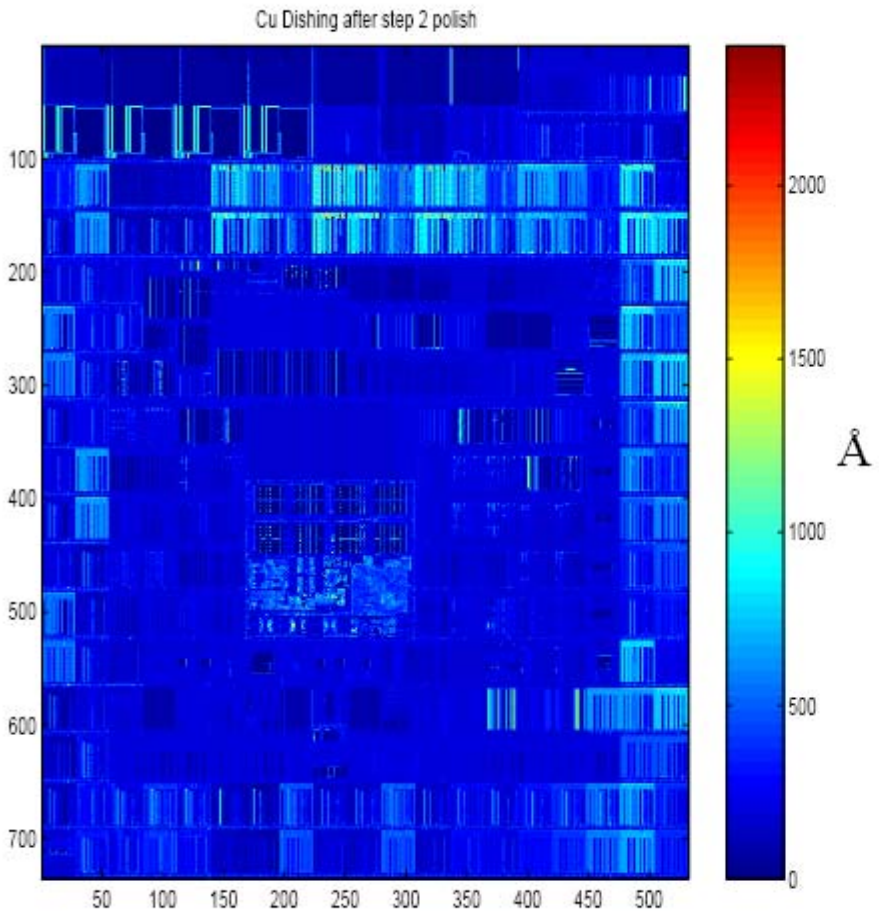


Effective Density Map Over Chip

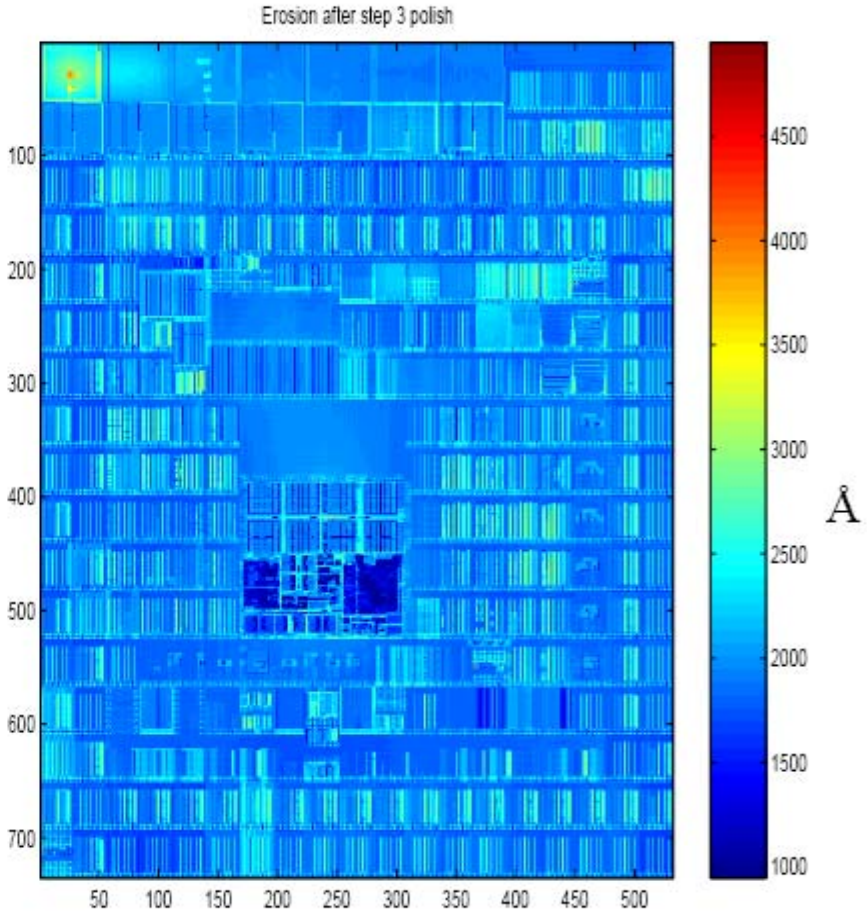


Ouma et al., *IITC '98*;
Smith et al., *CMPMIC '99*
Grillaert et al., *CMP-MIC '98.*

Chip-Scale CMP Simulation



Dishing after Step 2

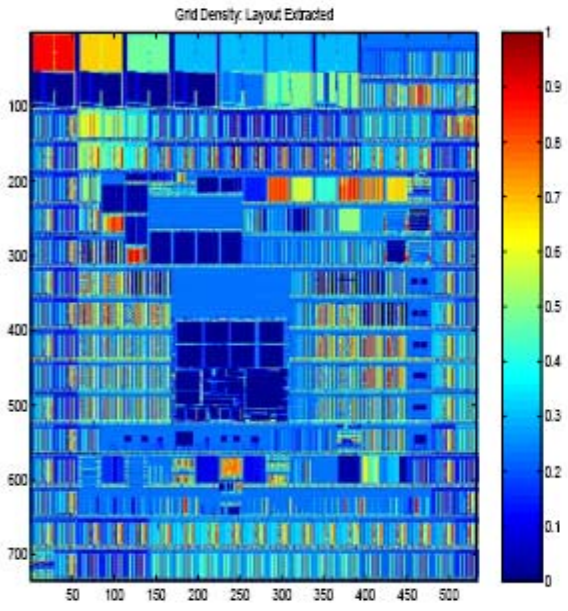


Erosion after Step 3

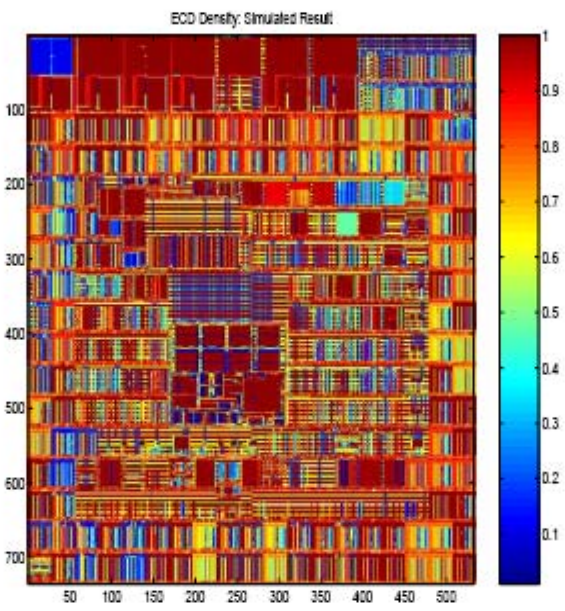
Process Optimization & Robust Design

Integrated Plating CMP Modeling

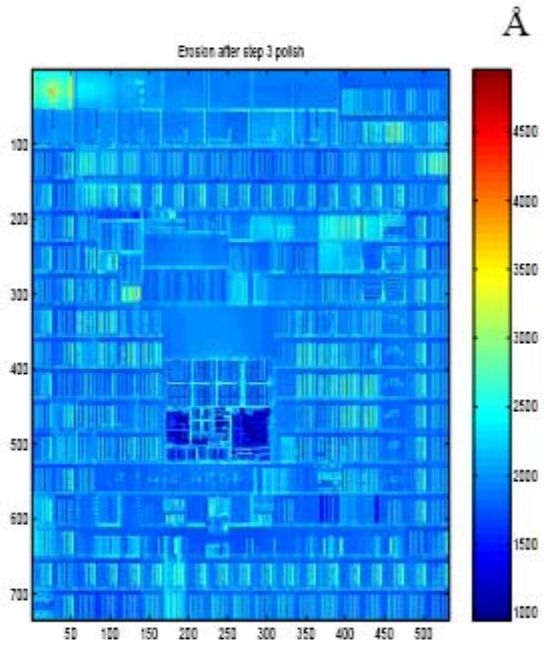
- Product Layout (Chip-Scale) Dependencies Captured
- Limited Process Parameters in Model
  - CMP polish time in each stage of the process



Local Layout Pattern Density



Post-Plating Raised Topography Density



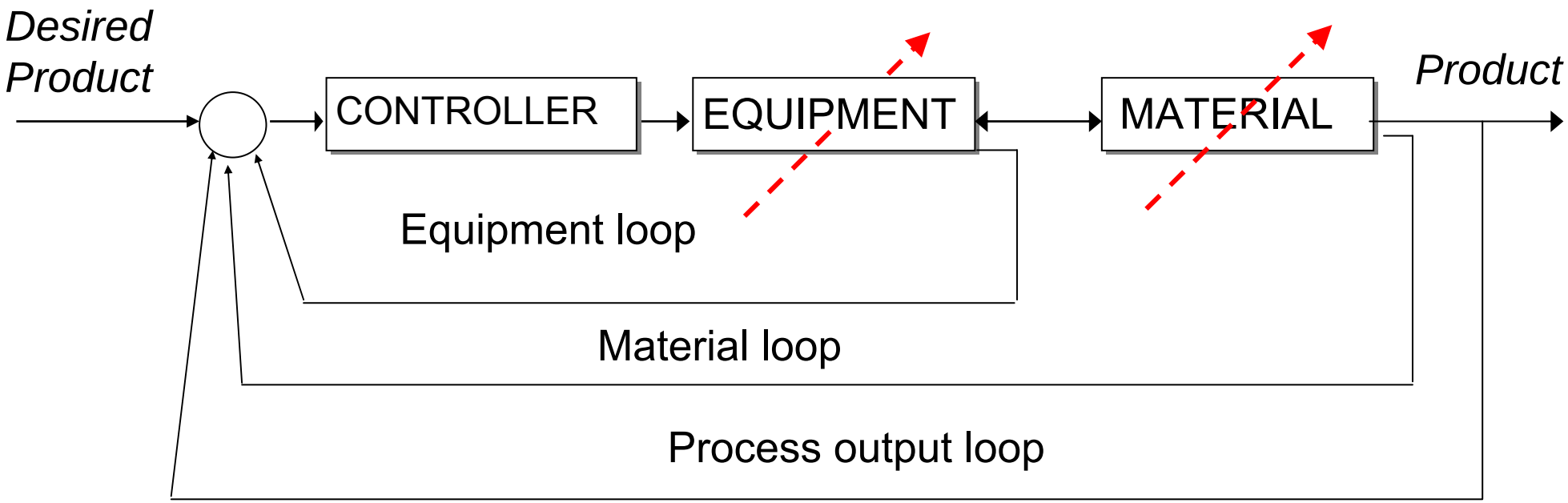
Post-CMP Erosion

Design Rule Generation

Image removed due to copyright restrictions. Please see Fig. 7 in Lakshminarayanan, S., et al. “Design Rule Methodology to Improve the Manufacturability of the Copper CMP Process.” *Proceedings of the IEEE International Interconnect Technology Conference* (2002): 99-101.

Feedback Control of Variation

The General Process Control Problem



Control of **Equipment**:

Forces,

Velocities

Temperatures, ...

Control of **Material**

Strains

Stresses

Temperatures,

Pressures, ...

Control of **Product**:

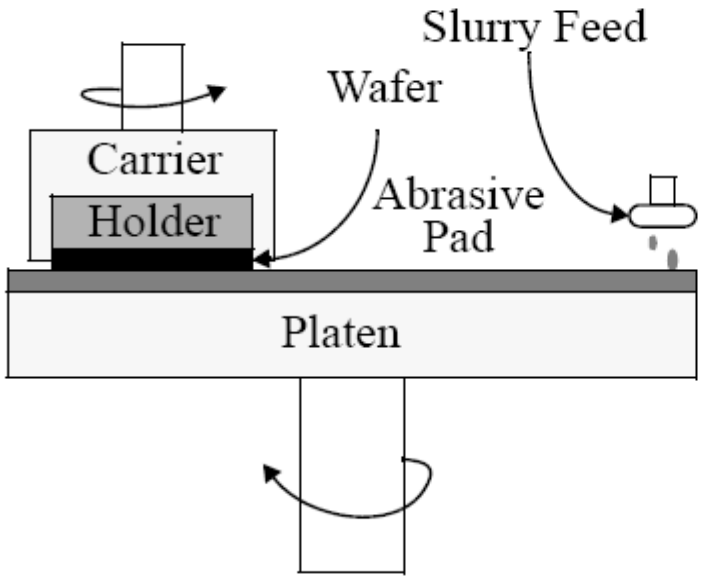
Geometry

and

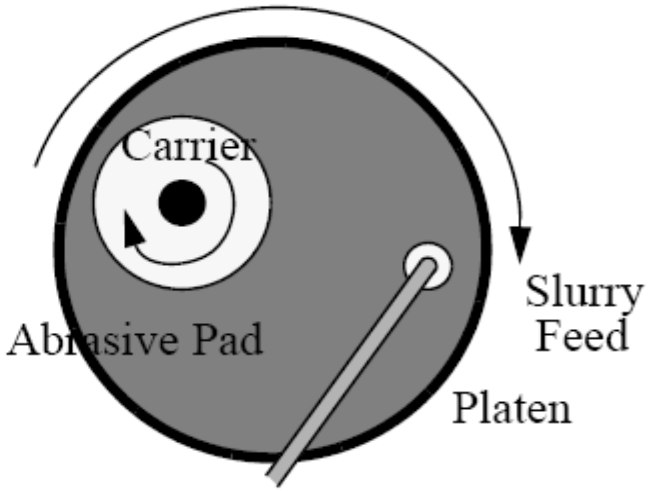
Properties

Chemical Mechanical Polishing

Side View



Top View

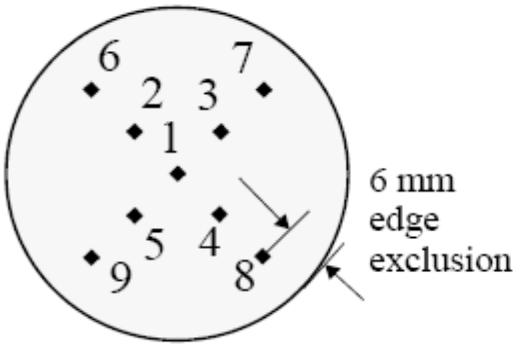


- CMP is critical to advanced IC interconnect technologies
- Key capability: "global" planarization of surface topography
- Active research in process, equipment, and sensor development

CMP Limitations and Control Challenges

- Limited understanding of the process
- Substantial drifts in equipment operation
- Lack of in-situ sensors

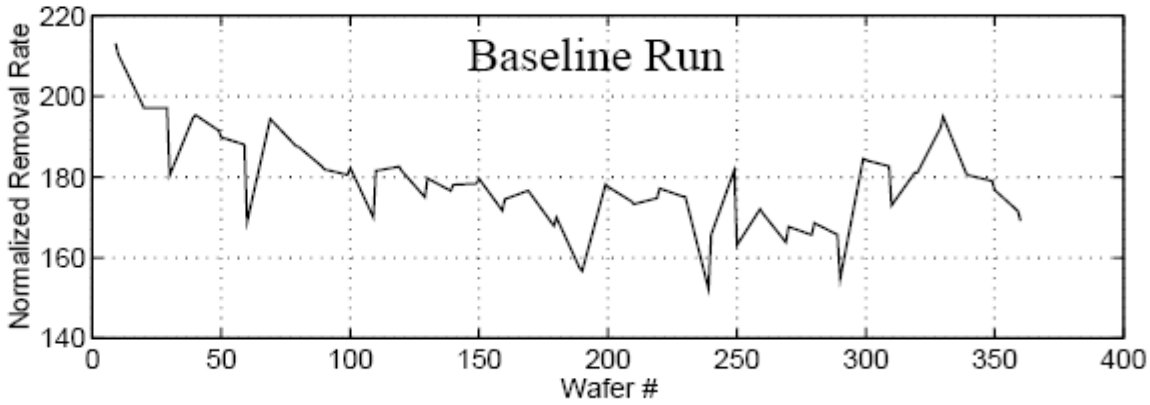
Blanket oxide wafer:

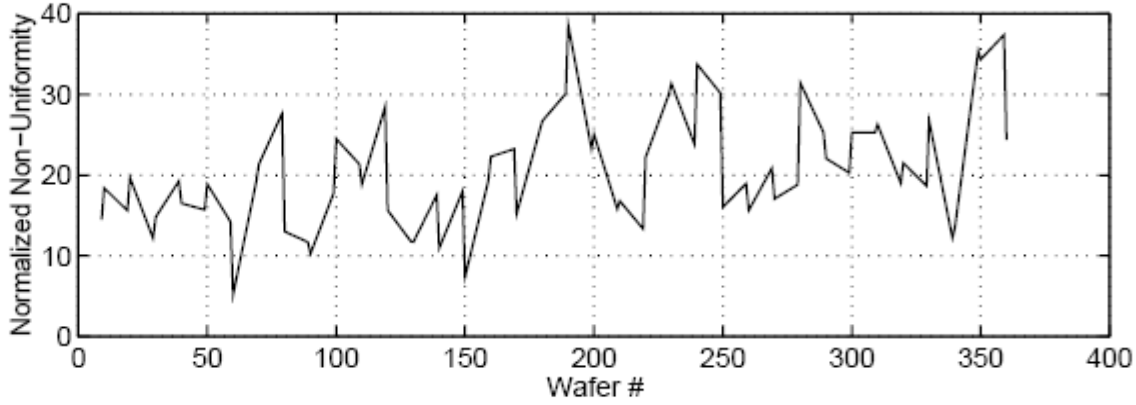


Targets:

Removal Rate

Nonuniformity





CMP Control Model Experiments

- Initial screening in seven factors to determine key control parameters
- Central composite DOE in four factors performed:

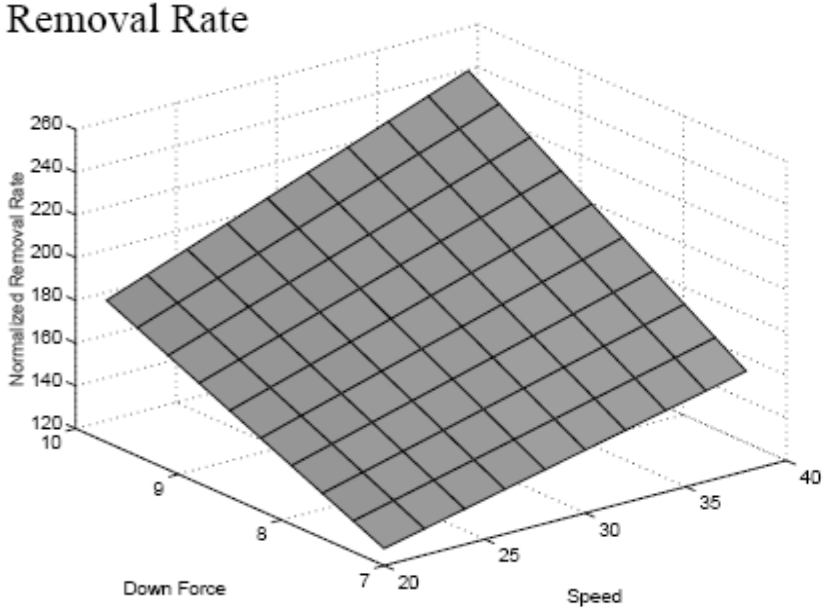
Factor	Lower Bound	Upper Bound
speed (rpm)	20	40
pressure (psi)	0	7
force (lb)	8	10
profile	-0.9	0.9

- Second order polynomial regression models fitted:
  - Removal rate -- R^2 of 89.7%
  - Nonuniformity -- R^2 of 76.9%

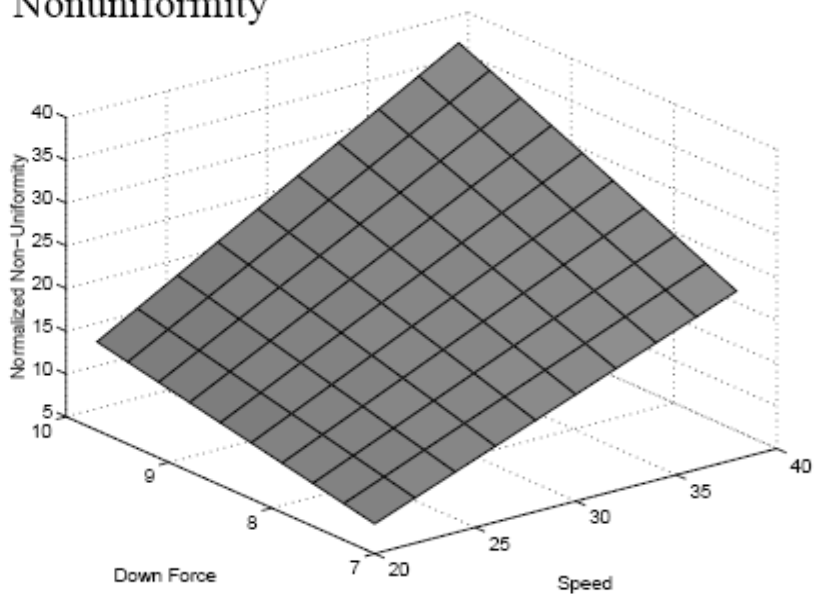
Control Model Development

- Response surfaces are nearly linear and well-behaved over operating region:

Removal Rate



Nonuniformity

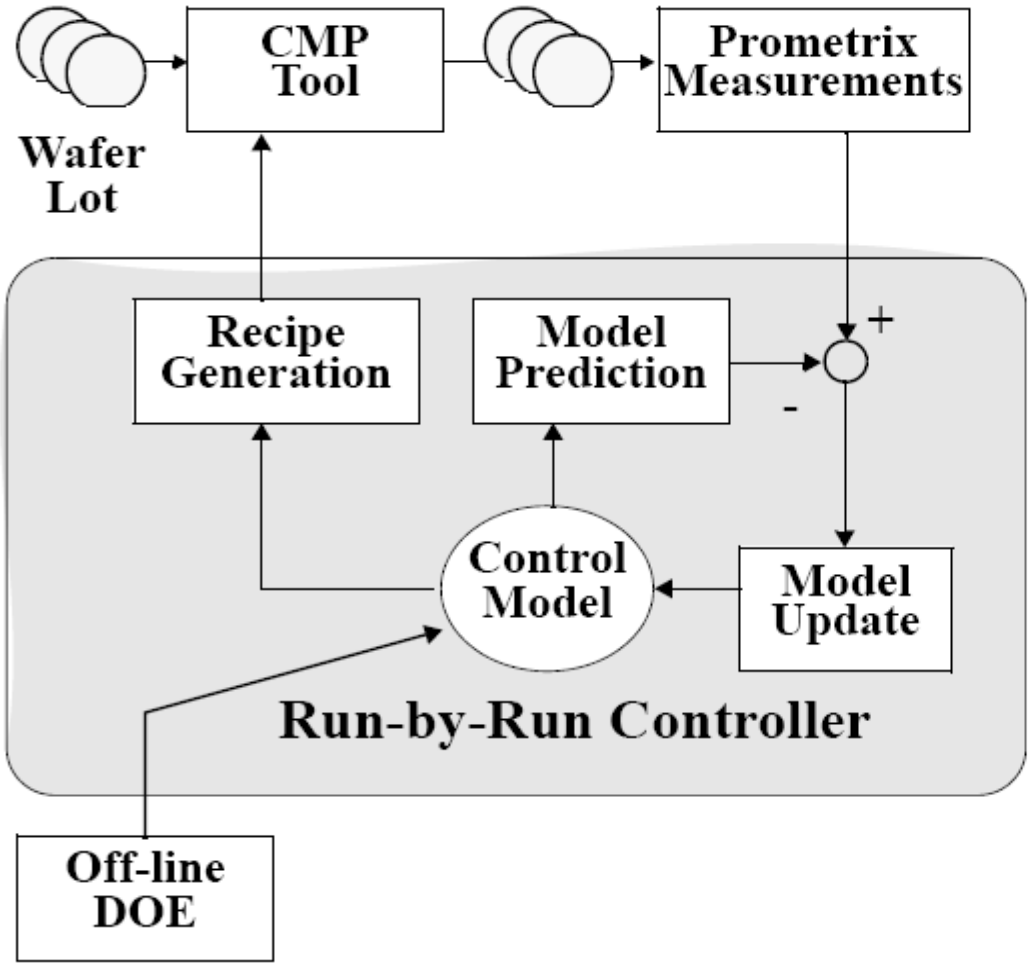


$$y = Ax + c$$

- Models Linearized for Control:

$$\begin{bmatrix} \text{removal rate} \\ \text{non-uniformity} \end{bmatrix} = A \begin{bmatrix} \text{speed} \\ \text{pressure} \\ \text{force} \\ \text{profile} \end{bmatrix} + c$$

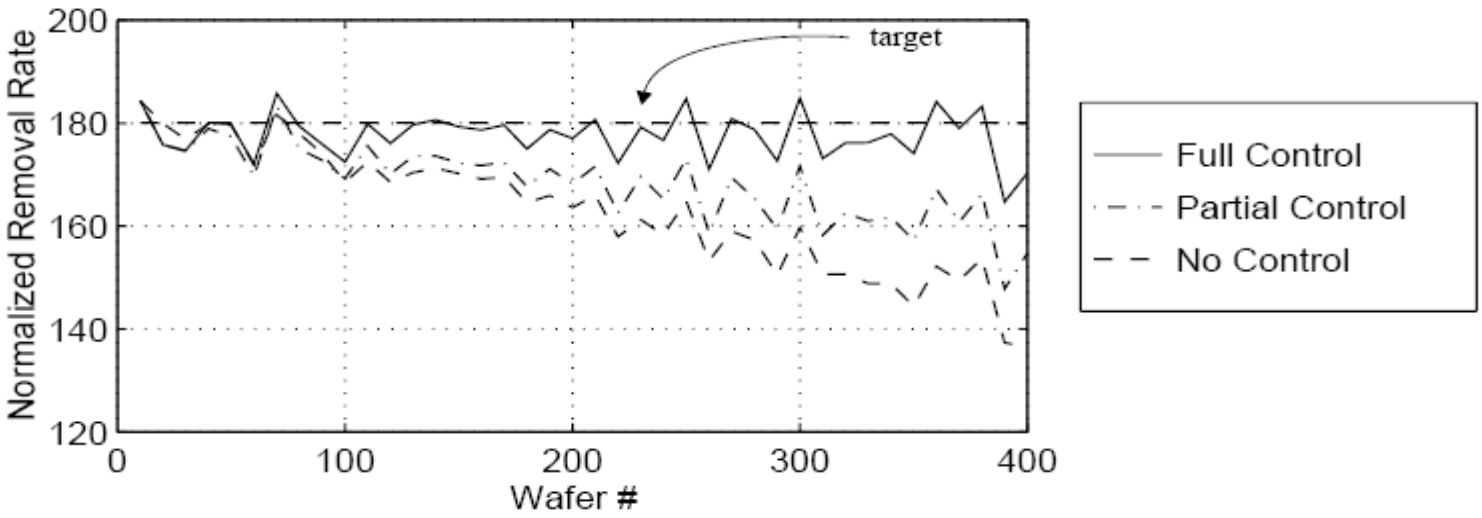
Run by Run Control Methodology



- Off-line experiments to build empirical response surface model of the process
- Select initial "optimal" recipe
- Planarize lots of 10 wafers each; measure wafers #9 & #10
- Adapt model based on measurements
- Generate new recipe using updated model to
  - achieve closest match to targets
  - achieve targets with smallest change in recipe

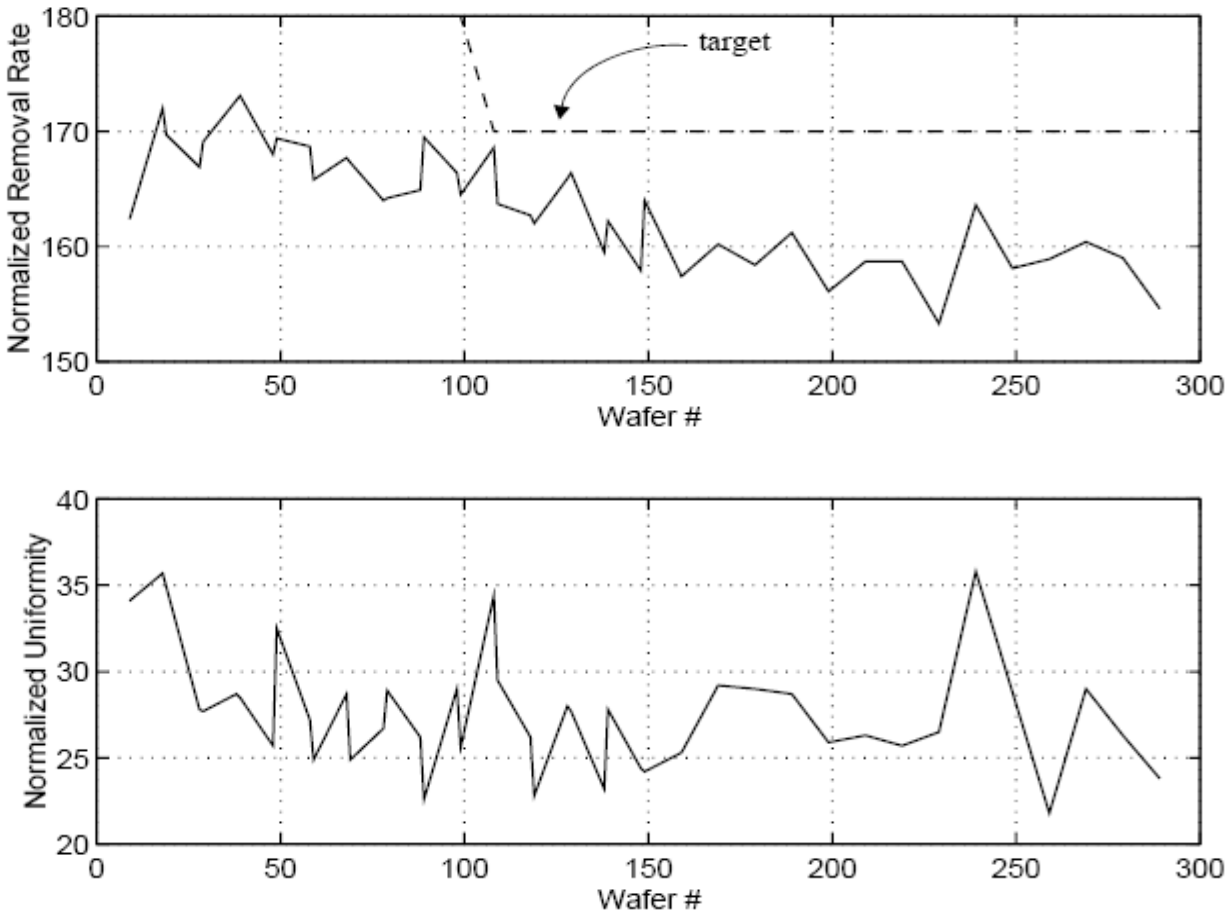
Control Algorithm Comparison - Partial vs. Full Model Update

- Partial Model Update: $c_t = \alpha(y_t - Ax_t) + (1-\alpha)c_0$
  - Corrects the *original* model based on last run -- (proportional control)
- Full Model Update: $c_t = \alpha(y_t - Ax_t) + (1-\alpha)c_{\{t-1\}}$
  - Corrects the *previous* model based on last run -- (EWMA update)
- Simulation



Experiment #1: Partial Model Update

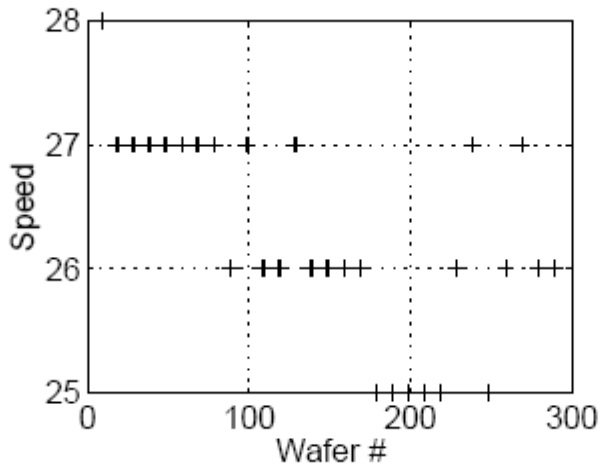
- Output Results:

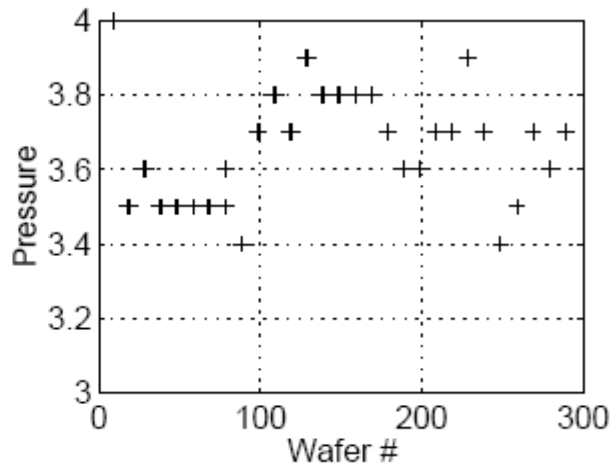


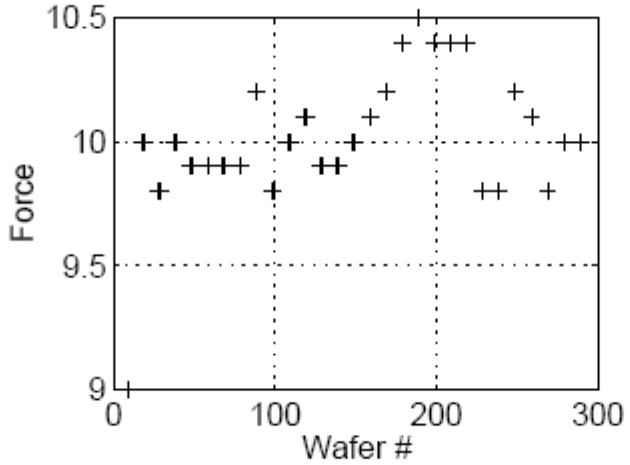
- Each new recipe is an improvement over *original* recipe, but...
- Controller unable to keep up with drift in the process

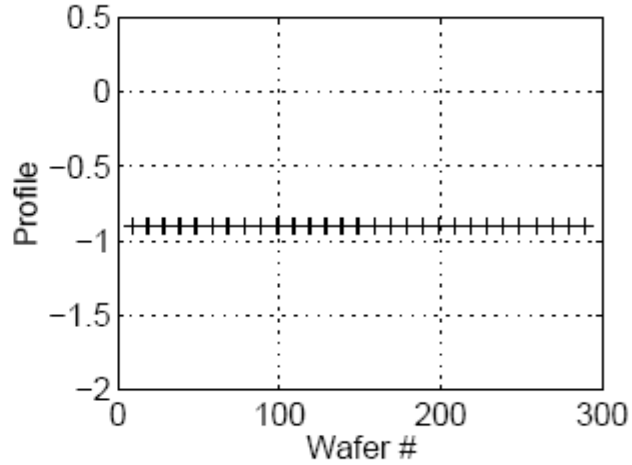
Experiment #1: Partial Model Update

- Control Inputs:





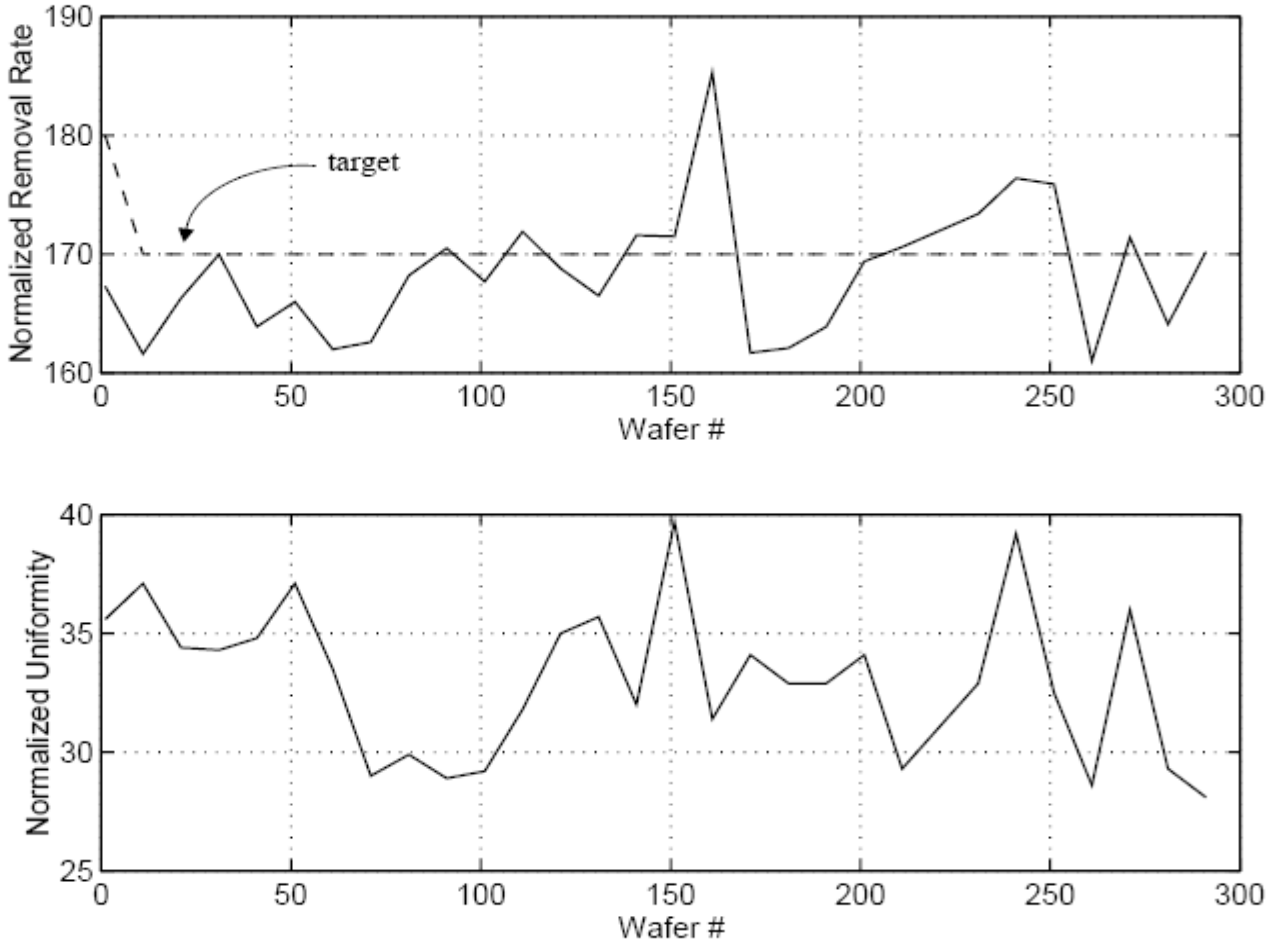




- Control inputs have not hit any limitations: failure is in model update

Experiment #2: Full Model Update

- Output Results:

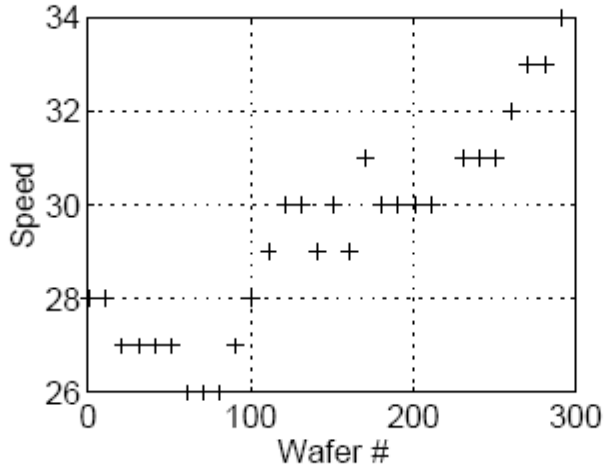


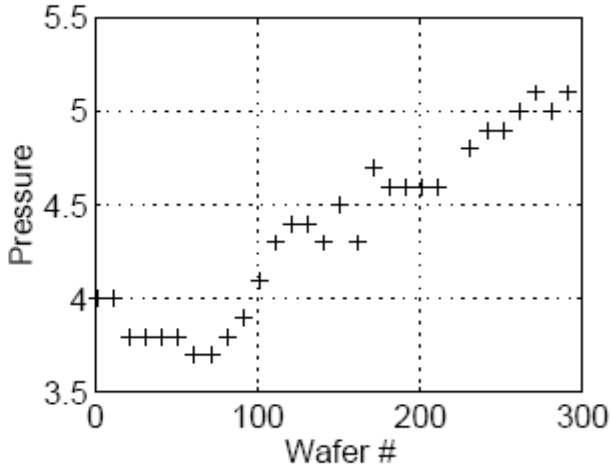
- Controller successfully compensates for drift in the process

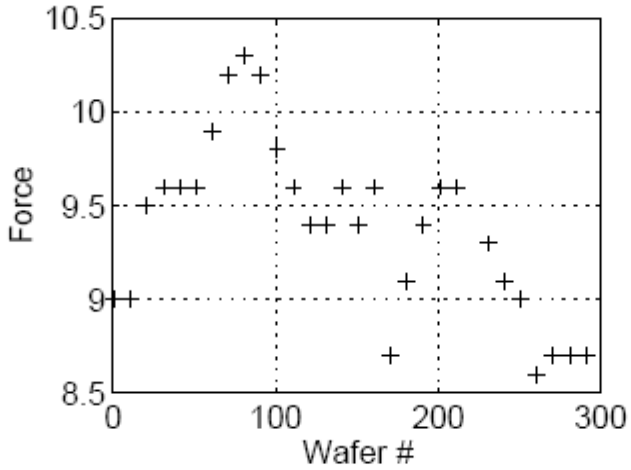
Experiment #2: Full Model Update

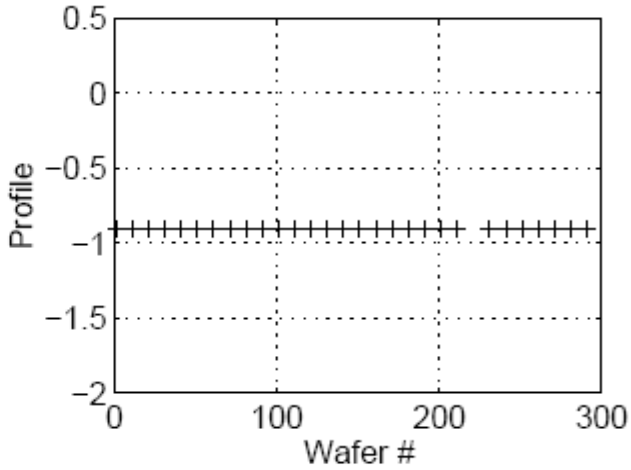
- Control Inputs:

Note: quantized control inputs produced by controller









- Controller produces increasingly aggressive control to compensate for drift

Summary

- The Semiconductor Fabrication Process
  - Manufacturing process control
- Types of Variation in Microfabrication
  - Defects vs. parametric variations
  - Temporal variations: wafer to wafer (run to run)
  - Spatial variations: wafer, chip, and feature level
- Preview of manufacturing control techniques
  - Statistical detection/analysis of variations
  - Characterization/modeling of processes & variation
  - Process optimization & robust design
  - Feedback control of process variation