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2.830J / 6.780J / ESD.63J Control of Manufacturing Processes (SMA 6303)
Spring 2008

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Massachusetts Institute of Technology

Department of Mechanical Engineering
Department of Electrical Engineering and Computer Science

2.830J/6.780J Control of Manufacturing Processes

Spring 2008

Assignment 5

Out 3/11/2008; due Thursday 3/20/2008

Part 1

May and Spanos problems 5.4, 5.5, 5.7, and 5.8

Part 2

Static random access memory (SRAM) 'cache' blocks form a crucial part of many integrated circuits, including the processors used in personal computers. Illustrated on the next page is a very simple memory block composed of an array of 256×256 cells, each cell capable of storing one bit of data (abstractly, a '1' or a '0'). To retrieve a particular 256-bit 'word' of data from the block, a signal is sent to one row of the array, causing each cell in that row to be connected to a pair of wires running parallel to the columns of the array. At the end of each of these pairs of wires is a highly sensitive differential amplifier that is designed to detect the value stored in the connected cell as quickly as possible. This scheme allows 256^2 bits to be accessed with just ~ 300 electrical connections to the block.

Here we consider the yield performance of the sense-amplifiers described above. An eager young circuit designer decides that he can enhance the SRAM's performance by reducing the gate lengths of the transistors in the differential amplifiers. Unfortunately, variability of the manufactured gate lengths leads to a 'mismatch' of the transistors within each amplifier and that mismatch becomes more pronounced as the nominal gate length is reduced. For the new design, Monte Carlo simulations suggest that the mismatch will be such that 0.5% of amplifiers cannot be relied upon to read data from the array correctly. The designer considers this fraction to be small enough, and sends the chip to be manufactured.

- (a) Assume that *each* of the columns in a given SRAM block must have a working amplifier for the chip to pass the testing phase. What is the functional yield if each chip has one SRAM block on it, and sense-amplifier failures are the only cause of functional yield loss?
- (b) What is the functional yield if there are four SRAM blocks on each chip and all four must be working for the chip to pass?
- (c) The circuit surrounding the SRAM block is changed so that the SRAM can be reconfigured and used if 25 or fewer of the columns have defective sense-amplifiers. Evaluate the functional yield now, if each chip has only one SRAM block.

