Microfabrication for MEMS: Part III

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* **With thanks to Steve Senturia, from whose lecture notes some of these materials are adapted.**

Outline

- Etching
- Wafer bonding
- Surface micromachining
- Process integration

Etching

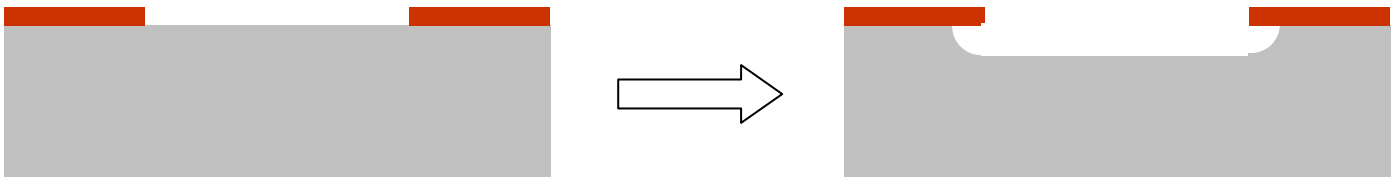
- **Wet etching**
  - **Isotropic**
  - **Anisotropic (for crystals only)**
- **Dry etching using plasma reactors**
  - **Isotropic "plasma" etching at relatively high gas pressures**
  - **Anisotropic "reaction-ion" etching at relatively lower gas pressures**
- **Sputter etching or ion-beam milling**
  - **Not very selective**
- **A useful reference (what etches what and how fast):**
  - **Williams, Gupta, and Wasilik, "Etch Rates for Micromachining Processing – Part II", JMEMS 12, 761-778 (2003).**

Considerations for etching

- Isotropic
  - Etch rate the same in all crystal directions
- Anisotropic
  - For wet etches, rate depends on crystal plane
  - For dry etches, directionality determined by process
- Selectivity
  - Etch rate of substrate vs. etch rate of mask
- Mask adhesion (for wet etching)
  - Increased etching along mask/substrate interface
- Temperature
  - Reaction rate limited?
- Stirring
  - Mass transfer limited?

Isotropic etching

- Etch rate is independent of orientation
- Isotropic etch profile
  - Assume a well-adhered mask with infinite selectivity
  - Mask undercut, rounded etch profile



- Applications:
  - Flow channels
  - Removal of sacrificial layers in surface micromachining

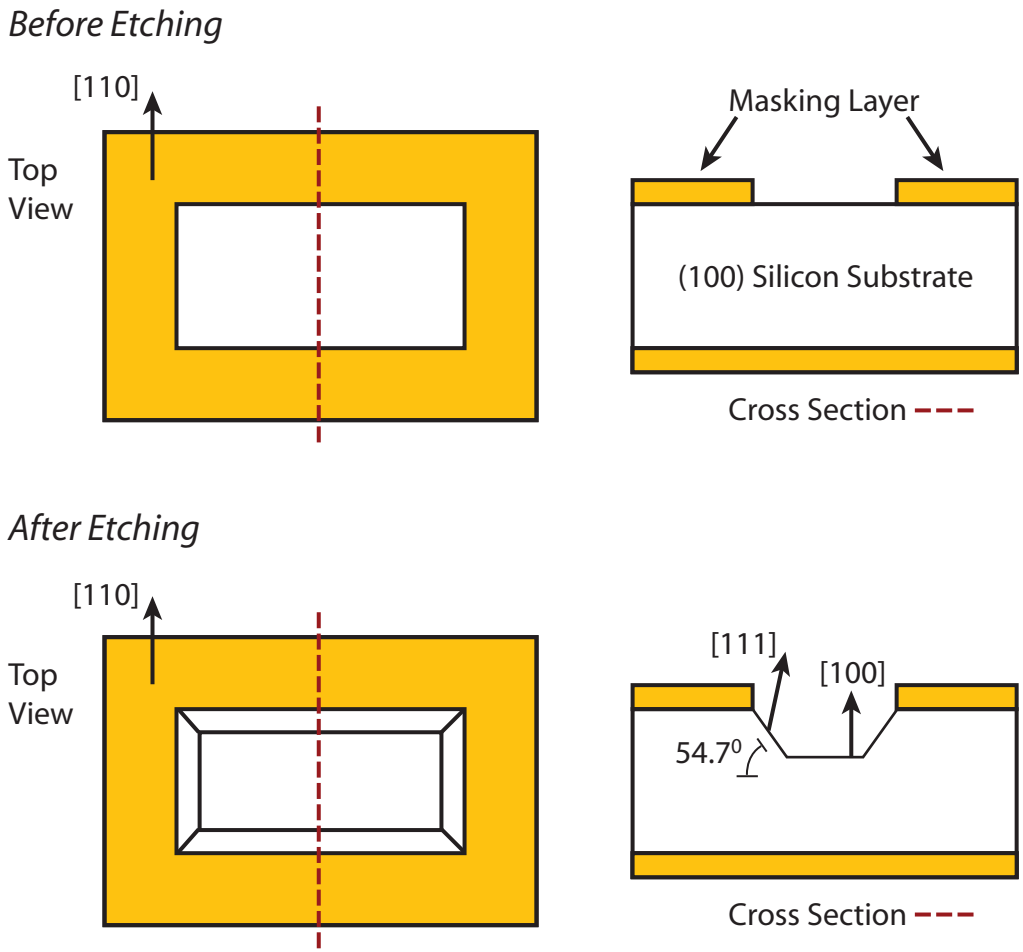
Isotropic etching

- Some wet etches:
  - Si — mixture of nitric, acetic, and hydrofluoric acid
  - SiO_2 — buffered HF (BOE), also HF vapor
  - SiN — hot phosphoric acid
  - PolySi — KOH
  - Al — PAN etch (phosphoric, acetic, nitric acids)
- Some dry etches:
  - Si — XeF_2 vapor
  - Organics — O_2 plasma
- Mostly clean enough for front end, with the exception of KOH, which is a contamination risk for very high T processes. XeF_2 vapor is often used as a final release etch.

Anisotropic wet etching

- Depends on having a single-crystal substrate
- The effect depends on the different etch rates of different exposed crystal planes
- Silicon etchants for which <111> planes etch slowly
  - Strong bases (KOH, NaOH, NH_4OH)
  - TMAH
  - Ethylene diamine pyrochatechol
  - Hydrazine

Making a Trench with KOH



> **A rectangular pattern is aligned to a [110] direction on a <100> silicon wafer**

Image by MIT OpenCourseWare.
Adapted from Figure 3.20 in: Senturia, Stephen D. *Microsystem Design*. Boston, MA: Kluwer Academic Publishers, 2001, p. 62. ISBN: 9780792372462.

Making a V-groove

- The previous etch is allowed to go to "termination", i.e. the slowing of etch rate when only {111} planes are exposed

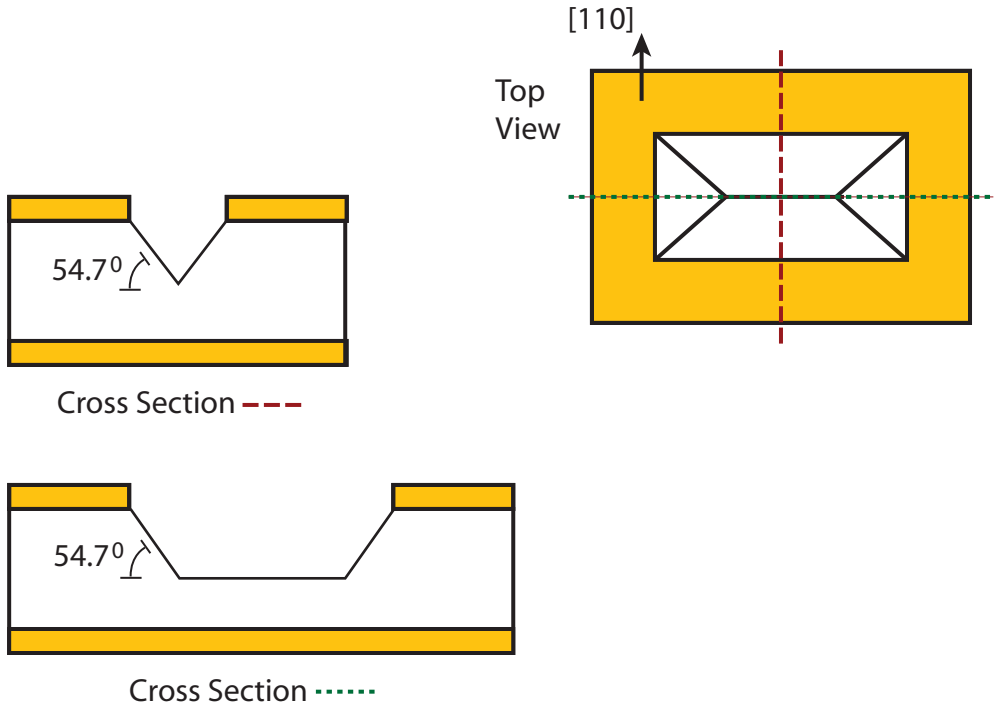
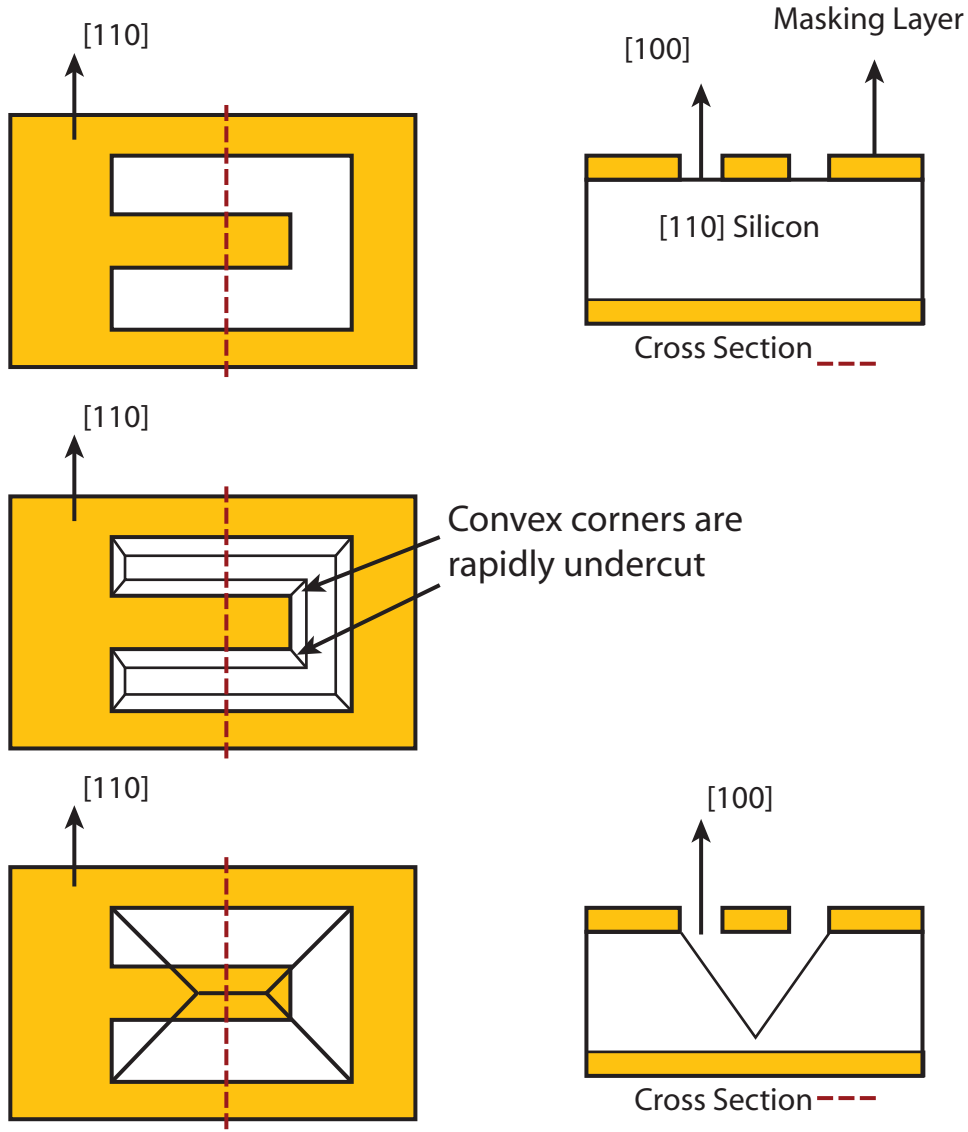


Image by MIT OpenCourseWare.
Adapted from Figure 3.21 in: Senturia, Stephen D. *Microsystem Design*. Boston, MA: Kluwer Academic Publishers, 2001, p. 63. ISBN: 9780792372462.

- Can also make a square, pyramidal hole

Convex corners

- Convex corners become undercut, as there is no single slow-etching (111) plane to stop on



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Adapted from Figure 3.23 in: Senturia, Stephen D. *Microsystem Design*
Boston, MA: Kluwer Academic Publishers, 2001, p. 64. ISBN: 9780792372462.

Corner Compensation

Image removed due to copyright restrictions.
Figure 3 on p. 143 in: Enoksson, Peter. "New Structure for Corner Compensation in Anisotropic KOH Etching." *Journal of Micromechanics and Microengineering* 7, no. 3 (September 1997): 141-144.

A common approach to corner compensation as shown in Enoksson, J. Micromech. Microeng. 7 (1997), 141-144.

- **To etch a convex corner with KOH, add extra material at corner**
- **Amount of material is chosen so that it will etch away just when the overall etch reaches the desired depth**
- **Extra material protects convex corner from attack**

Arbitrary shapes

- **Any mask feature, if etched long enough, will result in a V-groove tangent to the mask along <110> directions**

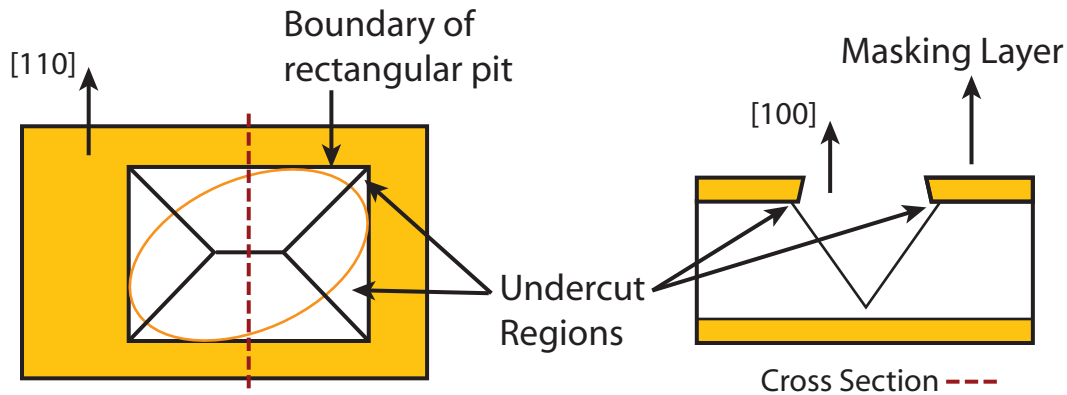


Image by MIT OpenCourseWare.
Figure 3.24 in: Senturia, Stephen D. *Microsystem Design*.
Boston, MA: Kluwer Academic Publishers, 2001, p. 64. ISBN: 9780792372462.

Misalignment

- **Misalignment of the mask relative to the [110] direction always results in a larger etched region**

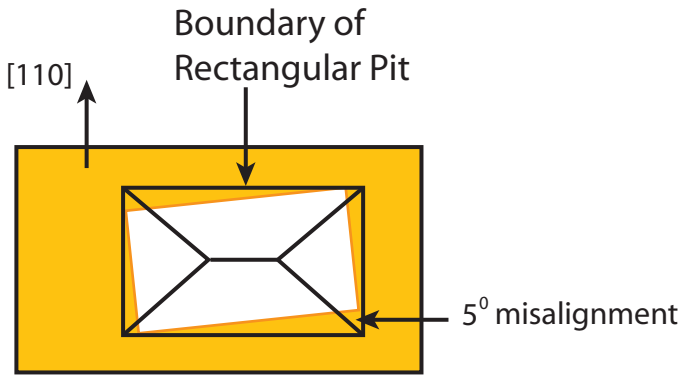


Image by MIT OpenCourseWare.
Figure 3.25 in: Senturia, Stephen D. *Microsystem Design*.
Boston, MA: Kluwer Academic Publishers, 2001, p. 65. ISBN: 9780792372462.

Selectivity and etch masks for KOH etches

- Deep etches are long – selectivity matters
- Mask must last long enough to bring the etch to completion
- Sidewall erosion must be at an acceptably slow rate
- Etch rate of {111} planes is finite but small
  - Condition-dependent, of order 400:1 for {100} rate/{111} rate
- Etch rate of mask
  - Si:SiO_2 selectivity about 100:1
  - Si:LPCVD SiN selectivity at least 1000:1
  - PECVD SiN not effective (low quality)
  - Don't use photoresist!

Etch stops

- When etching into a wafer to leave a specific thickness of material, it is necessary to have some kind of etch stop.
- Example: diaphragm pressure sensor
  - Termination on {111} planes? (V-grooves only)
  - Prayer and a stop watch?
    - Usually gives poor thickness control
  - Chemical etch stop
    - An unetched material, e.g. oxide or nitride
    - Heavily boron doped silicon, p+, as etch stop for strong bases

      (etches several orders of magnitude more slowly than lightly doped if concentration > 5 x 10^{19} cm^{-3})
  - Electrochemical etch stop

Image removed due to copyright restrictions.

Motorola

Dry (Plasma) Etching

- At reduced pressure, a glow discharge is set up in a reactive gas environment
- This produces
  - Ions that can be accelerated by the electric fields at the bounding edges of the plasma so that they strike the surface – these can be quite directional in their impact
  - Free radicals (uncharged) that can diffuse to the surface and undergo reaction
- Etching depends on reaction followed by creation of a gaseous byproduct which is pumped away

Applicability

- **Most materials can be plasma etched**
  - **Oxide**
  - **Nitride**
  - **Silicon**
  - **Most metals (not the noble metals)**
  - **Polymers**
- **The art is in achieving suitable selectivity both for masking layers and to layers that lie beneath the layer being etched**
  - **Known recipes (gas mixtures, plasma conditions) with desired selectivity**
  - **End-point detection is an important part of “best practice” when using plasma etching**

Shape

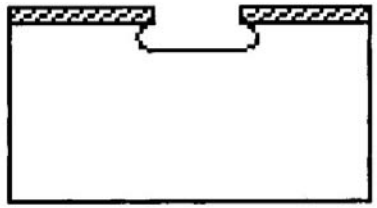
- The higher the pressure, the more isotropic the etch because reactants are scattered many times before reaching the surface (this is called “plasma” etching)
- To achieve directional anisotropy, one must go to low pressure to achieve long mean-free paths for the ions (this is called “reactive-ion etching” or RIE)
- Deep reactive ion etching is another thing altogether

Deep Reactive Ion Etching (The Bosch Process)

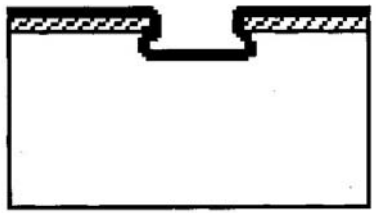
- Photoresist mask: selectivity about 50:1
- Oxide mask: selectivity > 100:1

1. Pattern photoresist

2. Reactive ion etch in SF_6



3. Deposit passivation (C_4F_8) (produces a teflon-like polymer)



4. Etch and repeat cycle (directional ions clear passivation from bottom only)

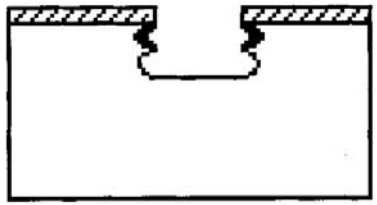


Figure 1 on p. 265 in: Chen, K.-S., A. A. Ayon, X. Zhang, and S. M. Spearing. "Effect of process parameters on the surface morphology and mechanical performance of silicon structures after deep reactive ion etching (DRIE)." *Journal of Microelectromechanical Systems* 11, no. 3 (2002): 264-275. © 2002 IEEE.

Depth depends on features and layout

- **Features of different width etch at different rates (recipe dependent)**

Image removed due to copyright restrictions.
Figure 3.28 in: Senturia, Stephen D. *Microsystem Design*. Boston, MA: Kluwer Academic Publishers, 2001, p. 70. ISBN: 9780792372462.

Multi-level Etching

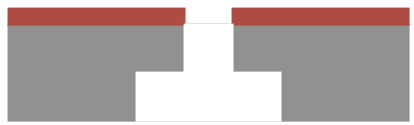
- Making multi level etches can be challenging
- For through etches with two different depths, simply etch from both sides of the wafer, with double-sided alignment

Pattern side 1

Etch side 1

Flip wafer and pattern side 2

Etch side 2



Multi-level Etching with Nested Masks

> Etching two sets of deep (> about 10 μm) features on the same side of the wafer requires a nested mask

1. Grow oxide mask

2. Define resist mask

3. Etch oxide to form mask

4. Strip resist; pattern with new resist mask

5. Etch to first depth

6. Strip resist mask

7. Using oxide as a mask, etch to second depth

8. Strip oxide mask

DRIE with Etch Stop

- SOI substrate
- Buried oxide acts as an etch stop
- Charging can lead to "footing"

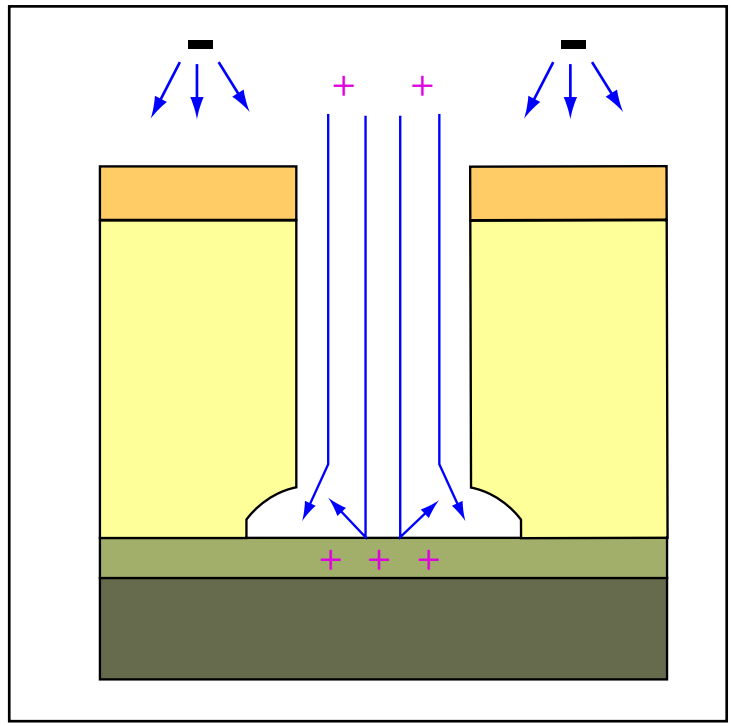


Image by MIT OpenCourseWare.

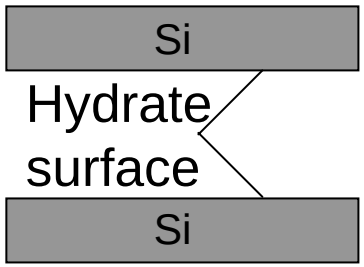
Outline

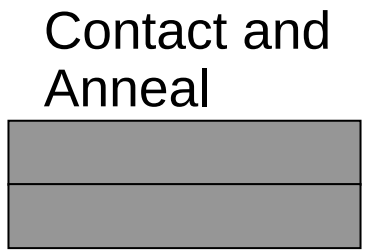
- Etching
- **Wafer bonding**
- Surface micromachining
- Process integration

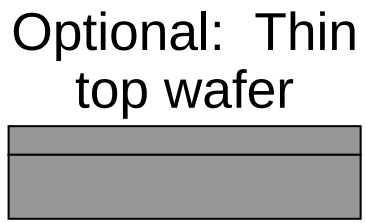
Fundamentals of Wafer Level Bonding

- **Two separate and distinct steps**
  - **The wafers are aligned to each other in a bond aligner with a possible alignment accuracy of one micron or less**
  - **The bond fixture is loaded into a vacuum bond chamber where the wafers are contacted together**
- **Three most prevalent types**
  - **Direct or fusion wafer bonding (high temperature, ~ 1000 C)**
  - **Anodic or field-assisted bonding, ~ 500 C**
  - **Bonding with an intermediate "glue" layer**
    - **Gold (thermocompression), ~ 300 C**
    - **Polymer or epoxy layer**

Direct Wafer Bonding







Spontaneous bonding reduces surface energy; compensates some strain energy cost.

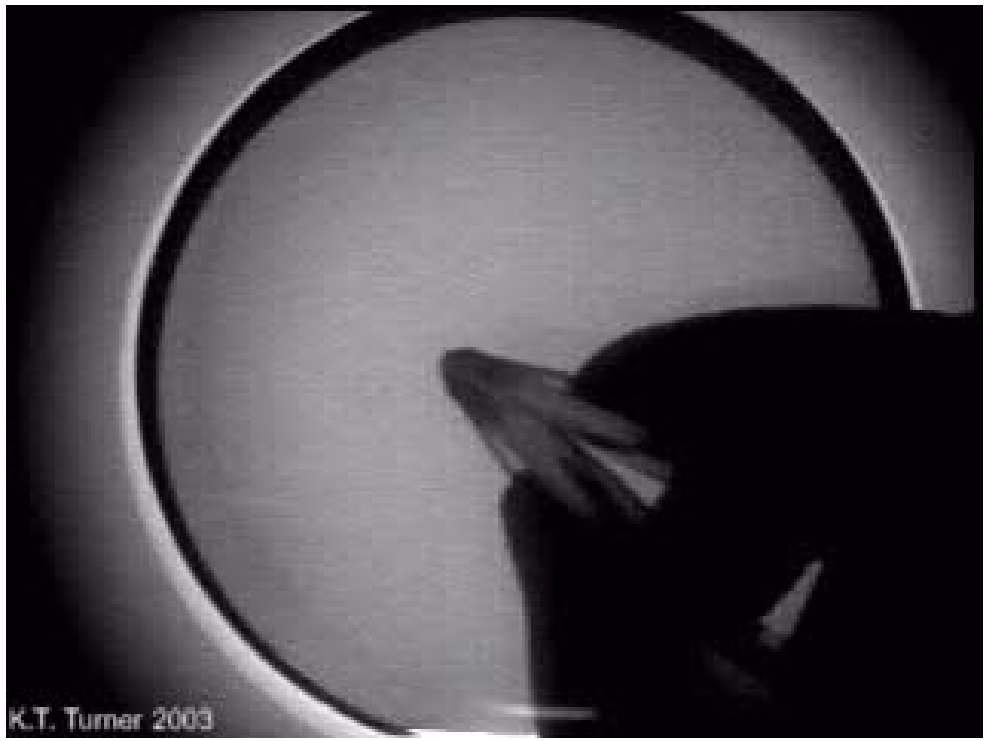
Si to Si, Si to oxide, oxide to oxide.

A high quality Si to Si bond can have bulk strength.

Image removed due to copyright restrictions.

DRIE and wafer bonding, London et al.

IR visualization of bond formation

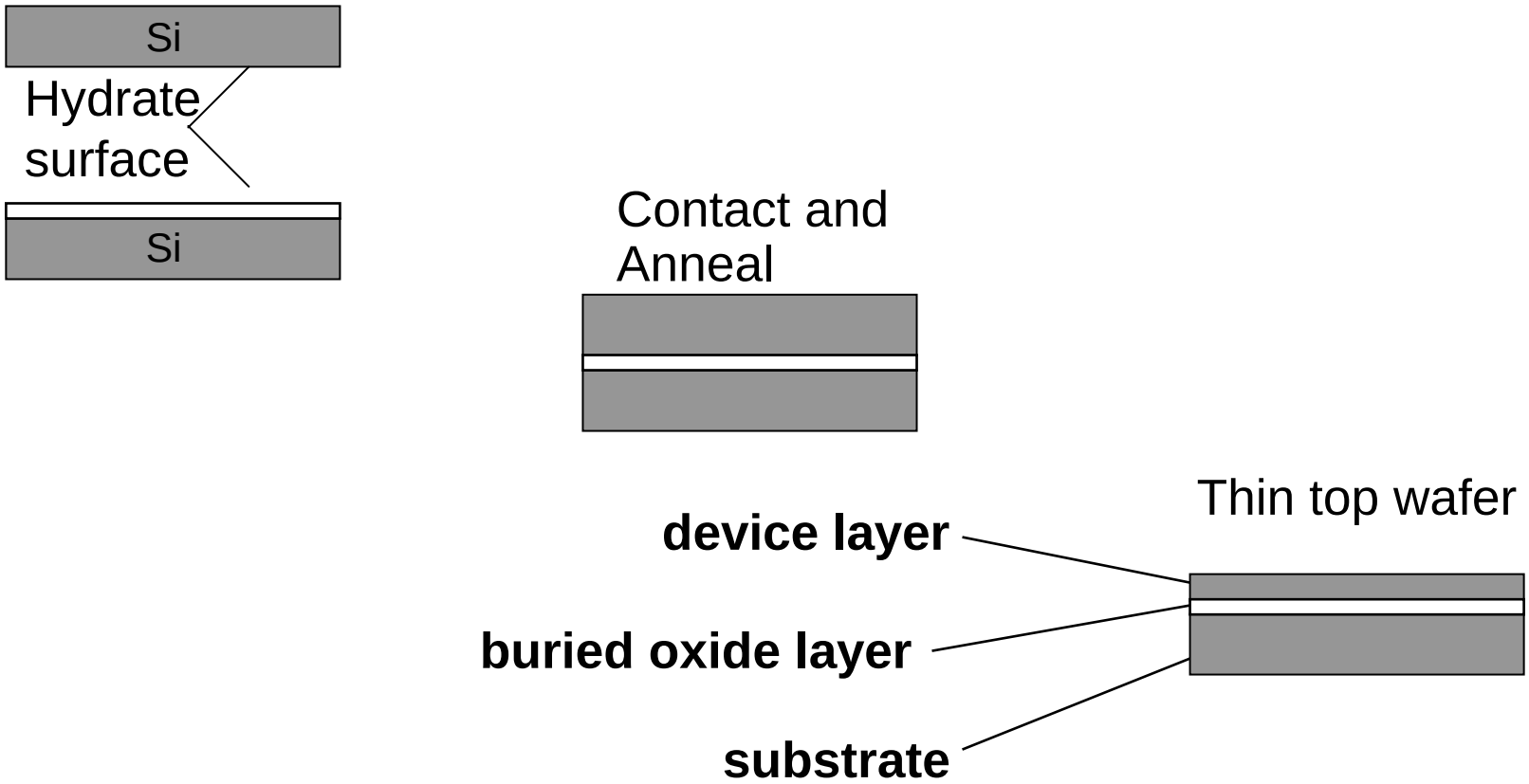


Kevin Turner, 2003.

Courtesy of Kevin Turner. Used with permission.

Silicon-on-insulator

> **Bonding to oxidized wafers is also possible, leading to silicon-on-insulator wafers**



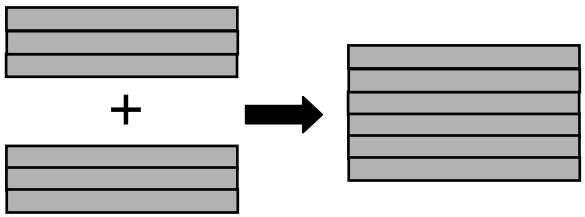
Wafer Geometry Impacts Bonding

- Spontaneous wafer bonding reduces surface energy
  - Two smooth, clean, perfectly flat wafers will bond spontaneously
- When wafers are not perfectly flat, bonding requires them to bend
  - Strain energy increases
- How far will two wafers bond?
  - Wafers bond until the surface energy reduction equals the strain energy cost
- Important factors
  - Wafer thickness
  - Radius of curvature
    - Wafer bow – innate or from stressed films
    - Waviness – locally greater curvature

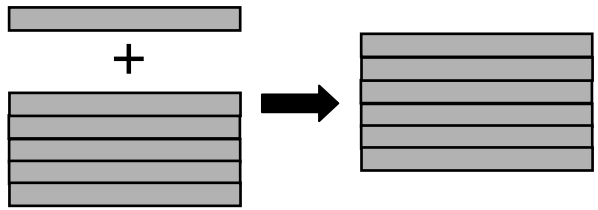
Wafer Geometry Impacts Bonding

> **Bonding order and strain energy**

- **For given total stack thickness, the strain energy accumulates fastest for wafers of equal thickness (goes as thickness cubed)**
- **K.T. Turner and S.M. Spearing, J. App. Phys., 92 (12) 2002, 7658-66.**
- **To bond n wafers, add them one at a time**



BAD



GOOD

> **Etched features**

- **Shallow etch hinders bonding (less interaction area)**
- **Deep etch aids bonding (less stiffness)**

Wafer bonding and yield

- Yield in MEMS can require a whole-wafer outlook, unlike IC processing
- A micron-scale defect can create a mm- to cm-scale defect
  - Amplification by wafer stiffness
- Can have a die yield of 100% on individual wafers and not get any devices if defects outside the die area prevent wafer bonding
- Cleanliness (particulates, organics) is critical to prevent defects; organics can outgas on anneal.
- Adjust process to minimize stiffness in bonding
  - At least one of the wafers should be thin (and therefore relatively pliable) when going into the bonding process

Anodic bonding

- The mobility of sodium ions in the glass drives anodic bonding
- The wafers are heated to temperatures of about 500C; a positive voltage (300 V – 700 V) applied to the Si repels sodium ions from the glass surface
- Suspectible to particulates, but less so than direct bonding
- Commonly used as a packaging step

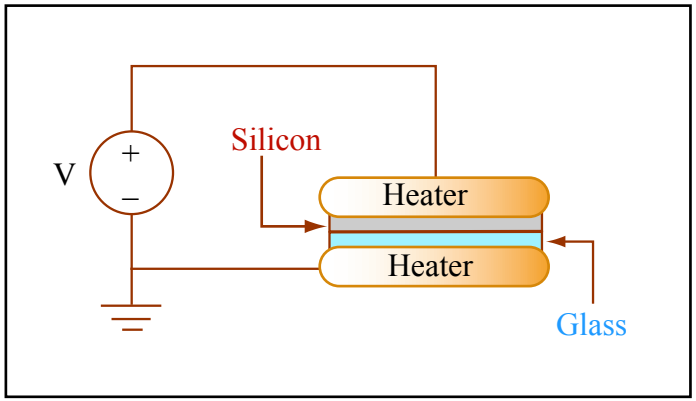


Image by MIT OpenCourseWare.

Designing process flows for cleanliness

- If you are planning to do a fusion bond, design your process flow to prevent exposure of bonding surfaces to junk
  - Cleanliness is a good idea for anodic bonding, too, but anodic bonding is less picky
- Some junk washes off easily, but some doesn't
- Example: deep reactive ion etching's passivation layer is reluctant to come off (ashing helps somewhat but isn't perfect)
- Work around: if possible, start your process by coating your wafer with a protective layer, like oxide. When you remove it right before bonding, it carries the junk away with it.

Outline

- Etching
- Wafer bonding
- Surface micromachining
- Process integration

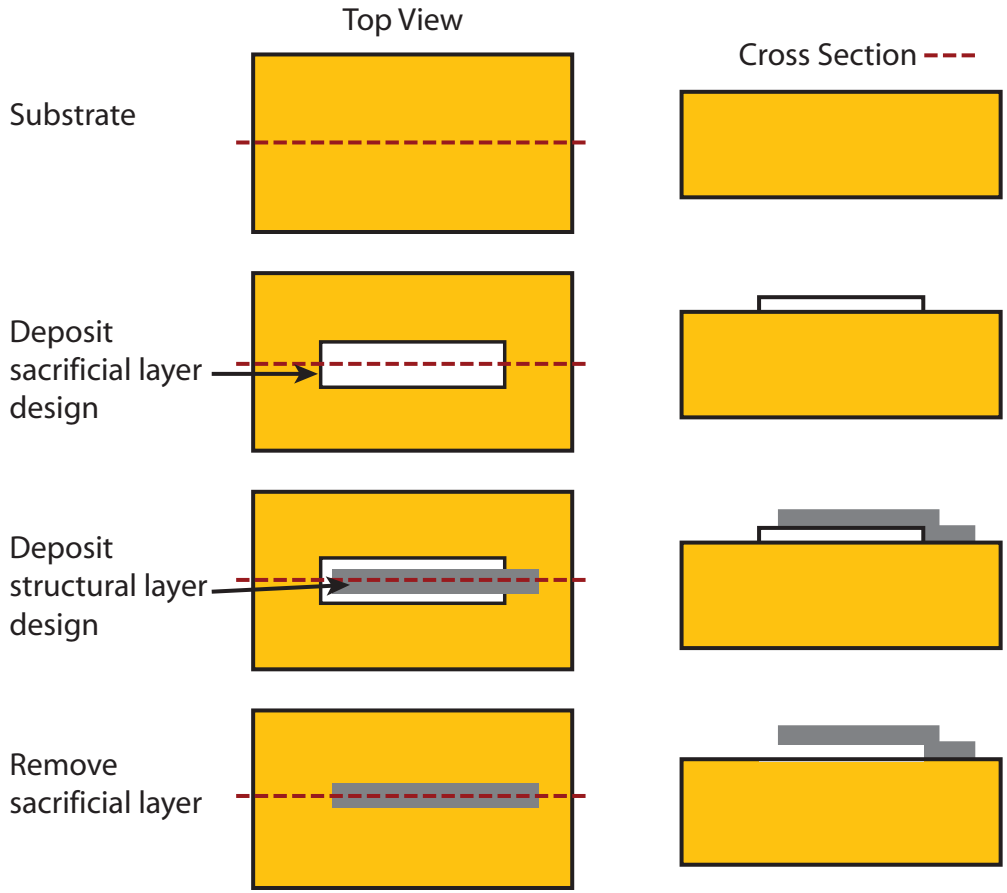
Surface Micromachining

- Surface micromachining refers to the selective removal of sacrificial layers beneath structural layers to create suspended structures
- Many materials choices possible
- Structural polysilicon and sacrificial PSG oxide is well-developed, fully characterized, and available as a foundry service
- Why use surface micromachining?
  - Complex multi-layer structures are possible without the need for wafer bonding
  - Structure thickness is controlled by thickness of deposited film, not by etch

Illustrating surface micromachining

> **Example**

- **Structural layer:**
  - » **polysilicon**
- **Sacrifical layer:**
  - » **Oxide**
- **Etchant**
  - » **HF**



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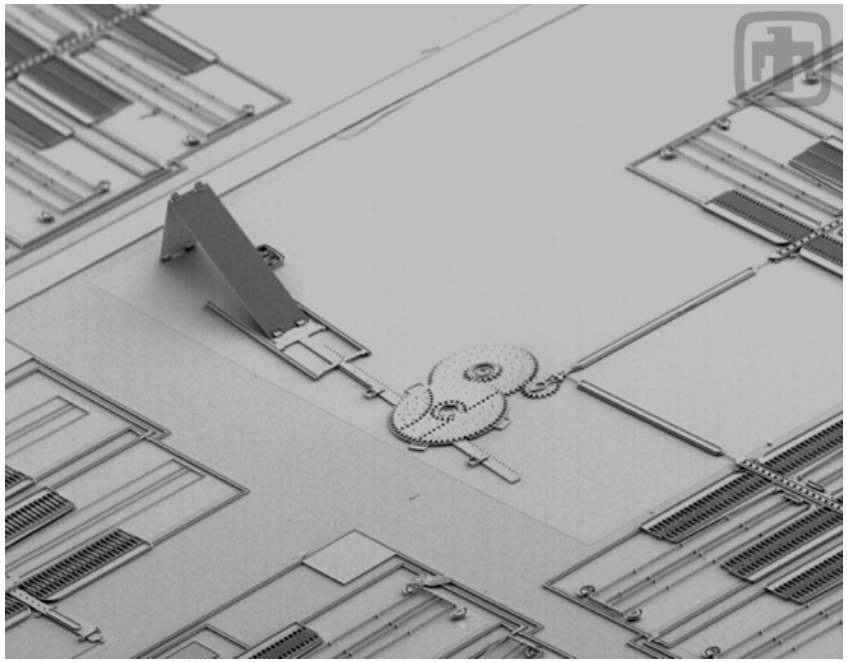
Adapted from Figure 3.19 in: Senturia, Stephen D. *Microsystem Design*. Boston, MA: Kluwer Academic Publishers, 2001, p. 59. ISBN: 9780792372462.

Surface Micromachining

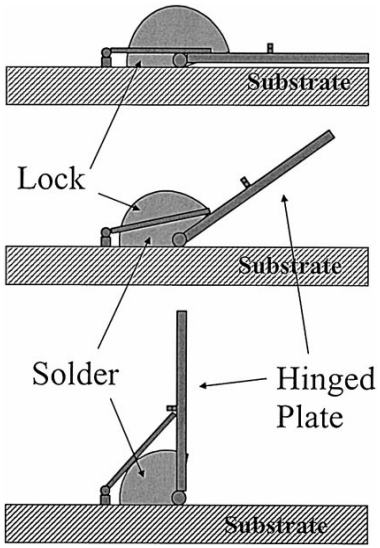


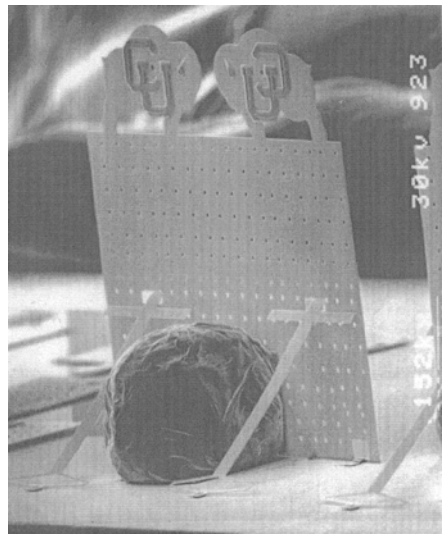
In-plane processing; potentially out of plane structures.

Courtesy of Sandia National Laboratories, SUMMiT™ Technologies, www.mems.sandia.gov

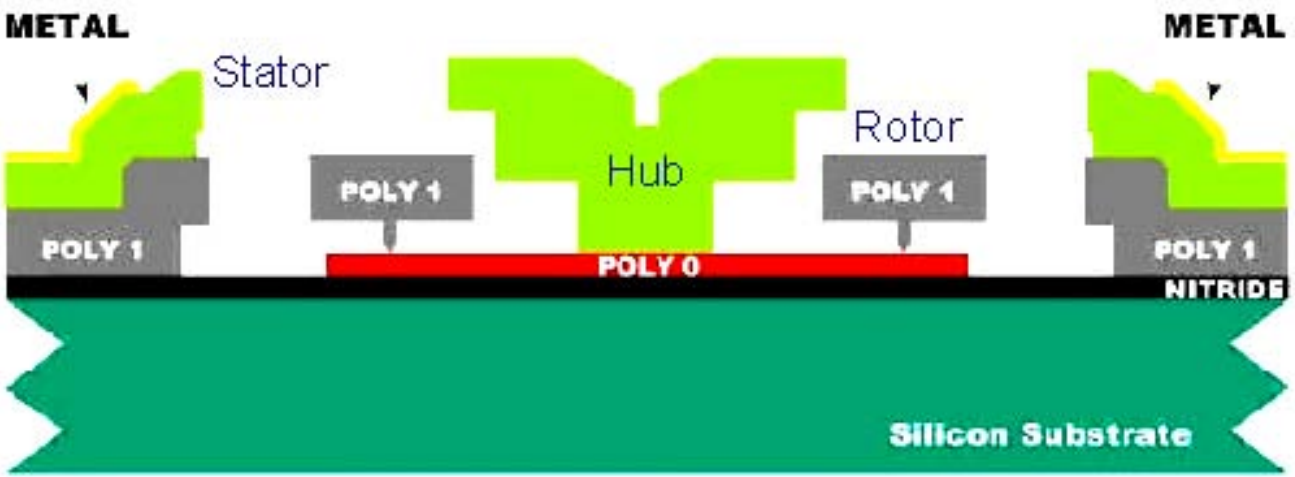
Solder assembly of surface micromachined parts

- Build surface micromachined parts
- Place solder over the joint
- Melt solder; surface tension bends part up until it hits limiter





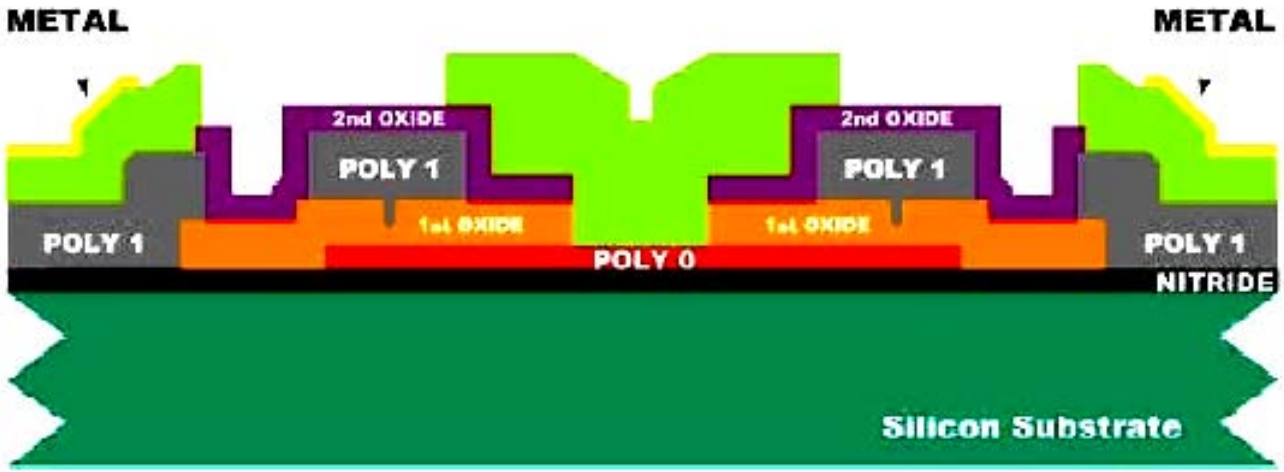
Introduction to MUMPs



Courtesy of MEMSCAP, Inc. Used with permission.

PolyMUMPs (Multi-User MEMS Process) is a three-layer polysilicon surface micromachining commercial process established in BSAC and now available from MEMSCAP.

MUMPs Process



Courtesy of MEMSCAP, Inc. Used with permission.

Cross section before sacrificial etch

- **Structural layers: Poly 0, Poly 1, Poly 2**
- **Sacrificial layers: Oxide 1, Oxide 2 (phosphosilicate glass)**
- **LPCVD nitride acts as passivation, electrical isolation layer**

MUMPS Process: Step 1

Courtesy of MEMSCAP, Inc. Used with permission.

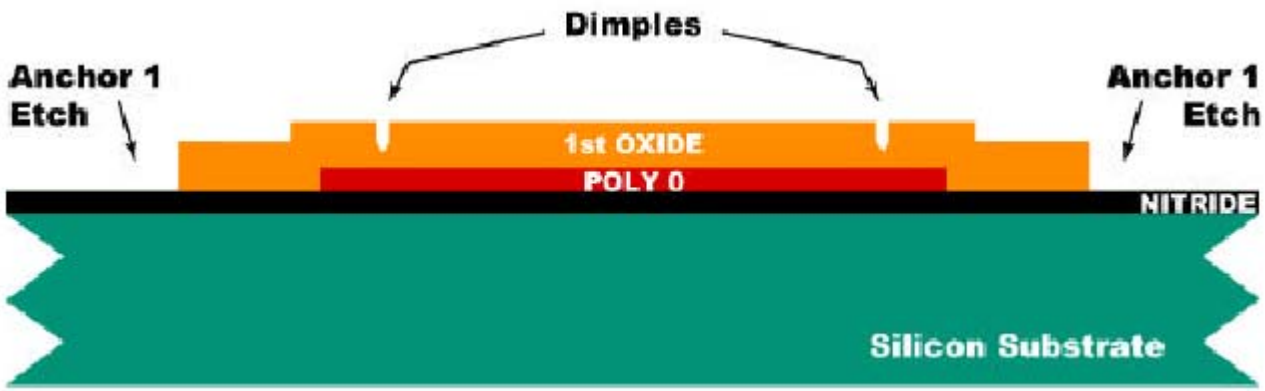
- 4" 100 silicon wafers, 1-2 Ω resistivity
- 600 nm LPCVD Si_3N_4
- 500 nm LPCVD polysilicon (Poly-0)
- Lithography poly-0 (Hole 0) and RIE poly-0

Step 2

Courtesy of MEMSCAP, Inc. Used with permission.

- 2.0 μm LPCVD PSG (oxide-1) and 1050 °C anneal
- Lithography Dimples and RIE PSG (750 nm)

Step 3



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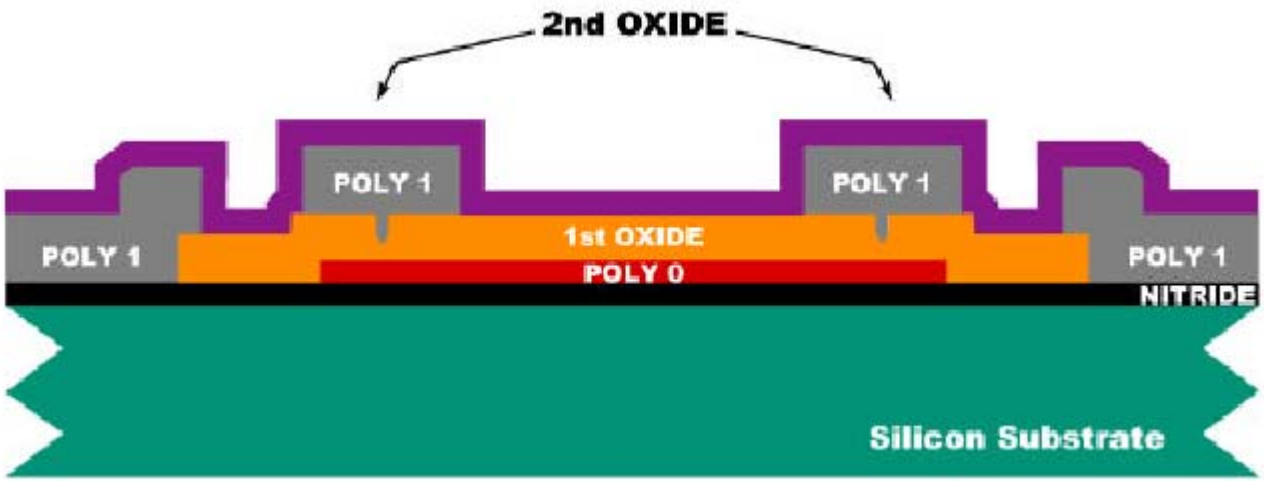
❑ **Lithography Anchor1 and RIE PSG**

Step 4

Courtesy of MEMSCAP, Inc. Used with permission.

- 2.0 μm LPCVD polysilicon (poly-1)
- Lithography Poly-1 (Hole 1) and RIE poly-1

Step 5



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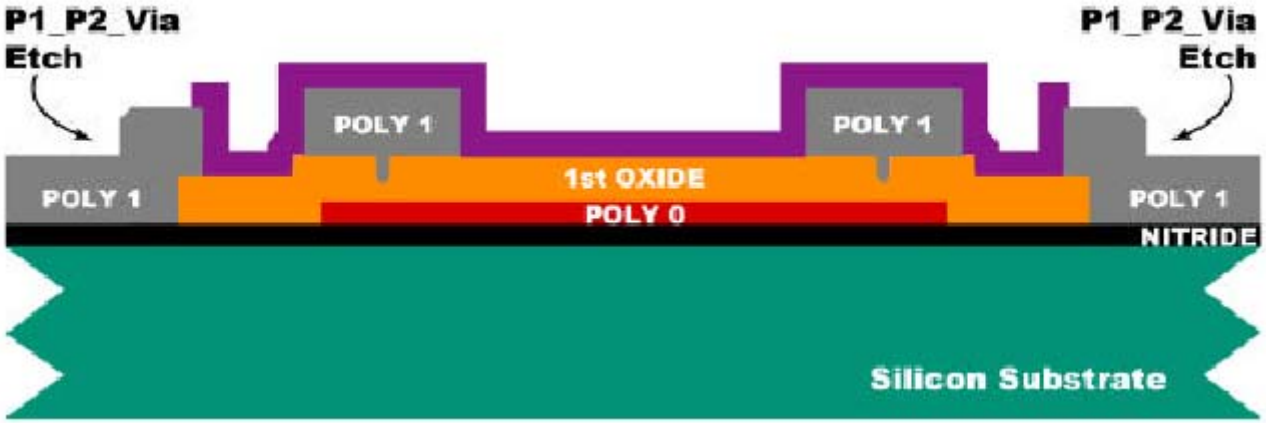
- **0.75 μm LPCVD PSG(oxide –2) and 1050 °C anneal**

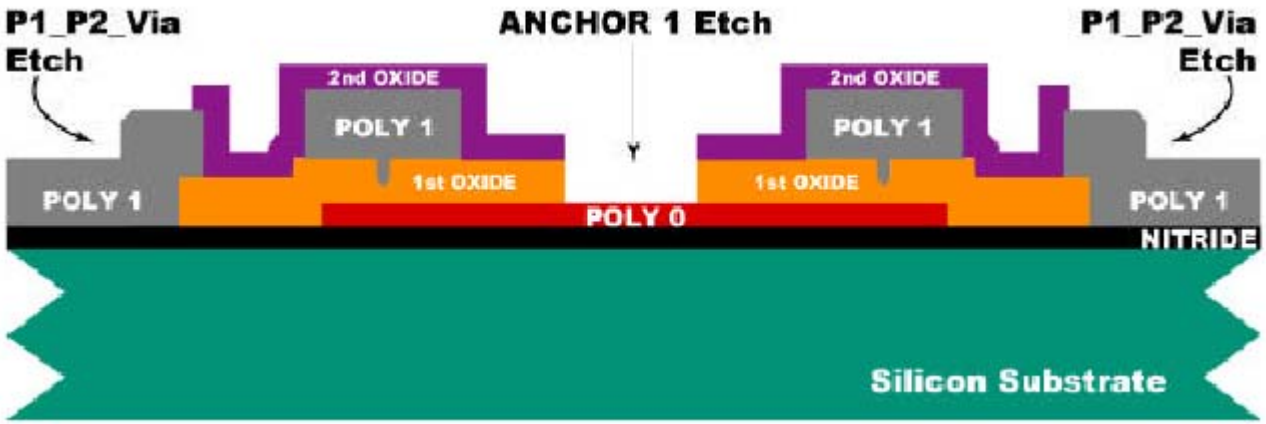
Step 6



Courtesy of MEMSCAP, Inc. Used with permission.

- **Lithography poly 2-poly1-via and RIE PSG (oxide 2)**

Step 7



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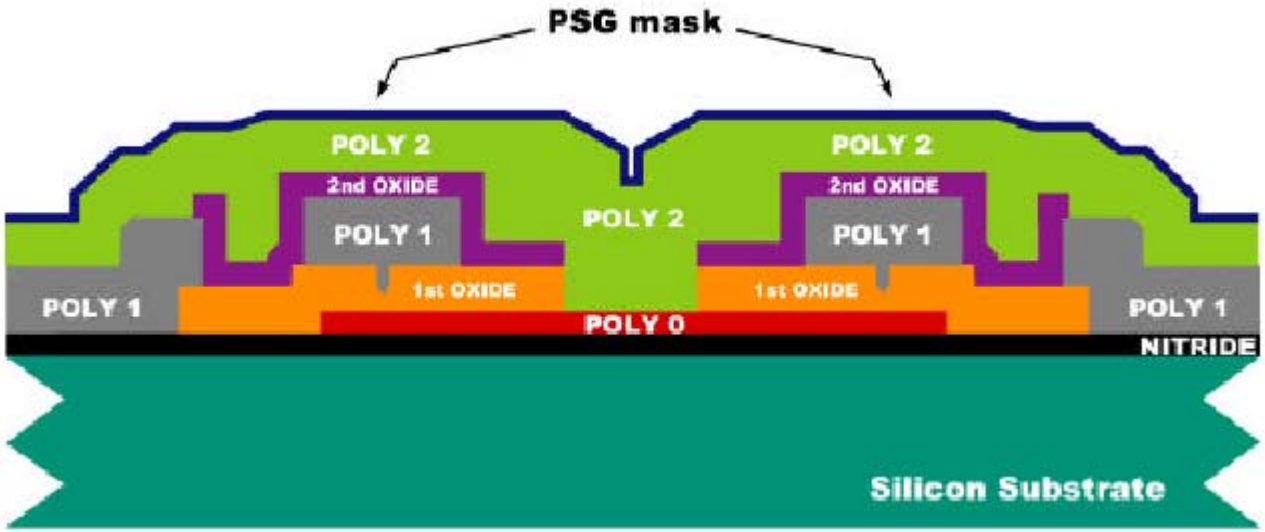
- Lithography **Anchor 2** and RIE PSG (oxide-2 and oxide-1)

Step 8



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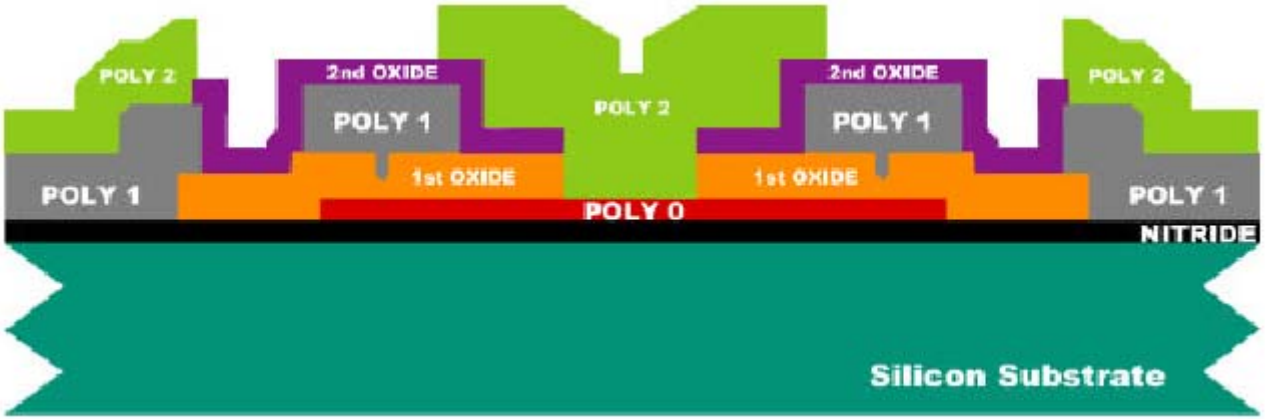
- 1.5 μm LPCVD polysilicon (poly-2)

Step 9



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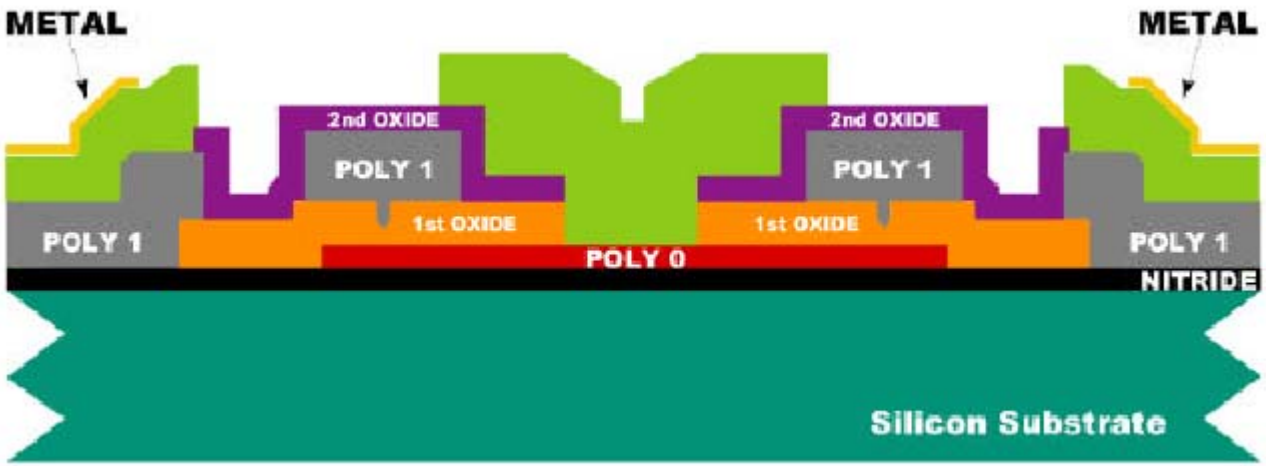
- Lithography poly-2 (Hole 2) and RIE poly-2

Step 10



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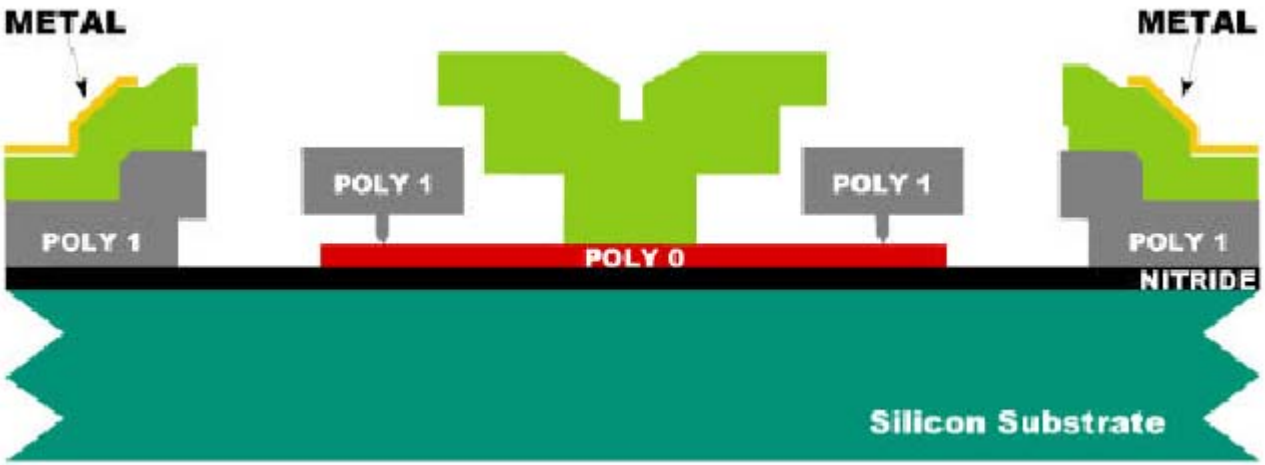
- 0.5 μm Cr/Au evaporation (Metal)
- Lithography Metal (HoleM) and lift off

Step 11



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Releasing

- 1.5-2 min 49% HF sacrificial oxide etch at room temp.
- CO_2 critical point drying

Limitations of Surface MM

Images removed due to copyright restrictions.

Stiction

- **Permanent adhesion between movable structures or structure and substrate**
- **Caused mainly by van der Waals forces due to hydrogen content or moisture on surface and close proximity of movable structures (due to thin films used)**

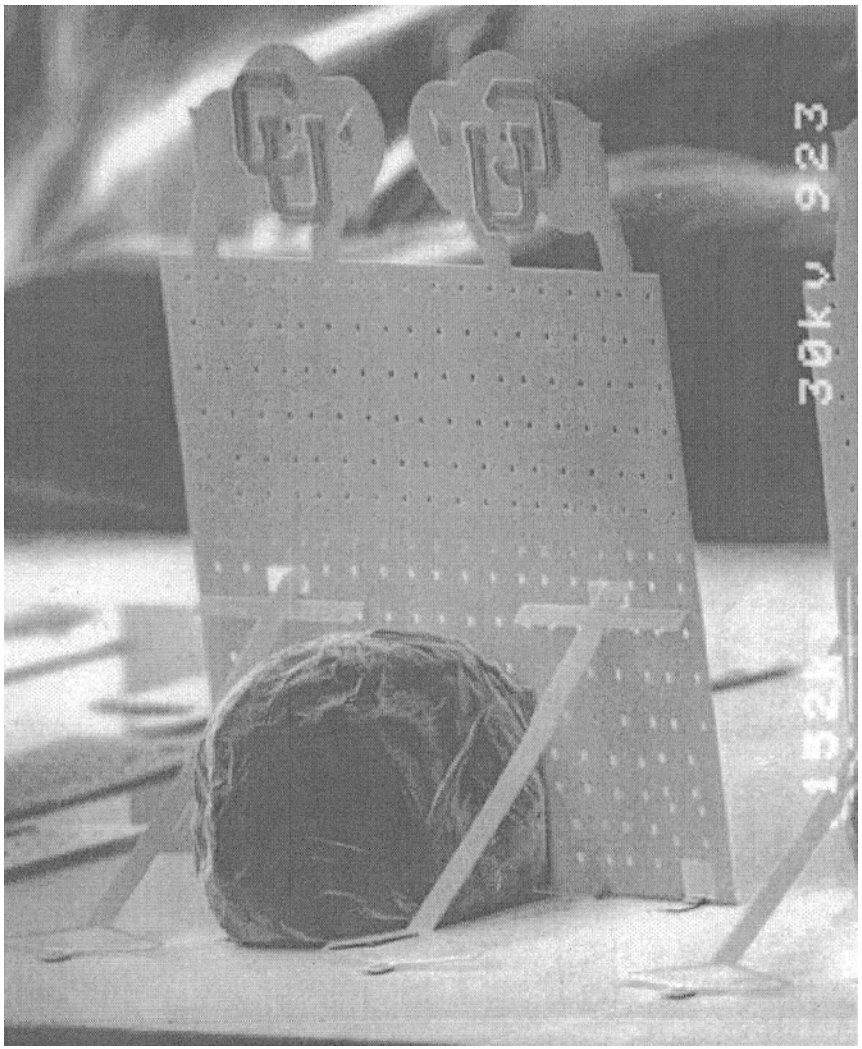
Dealing with stiction

- **Thin structures are susceptible**
  - **Deposited films**
  - **Narrow, deep-etched structures**
- **Prevention is key**
- **Options**
  - **Low surface tension liquid rinse after sacrificial etch**
  - **Surface roughening or surface coating (hydrophobic)**
  - **Critical point CO_2 or sublimation drying to prevent meniscus formation**

One release recipe

- Acetone soak to remove photoresist (30 min)
- Isopropanol soak to remove acetone (30 sec)
- Rinse in water to remove isopropanol (1 min)
- Soak in 49% HF (3:30 min)
- Soak in 4:1 methanol/water (9 min)
- CO_2 supercritical release. Liquid CO_2 is used to flush the methanol. The CO_2 is then heated and will subliminate around 35 °C.

HF only removes the oxide that it can reach



Holes in plates are important!

Figure 11 on p. 243 in Harsh, K. F., V. M. Bright, and Y. C. Lee. "Solder Self-assembly for Three-dimensional Microelectromechanical Systems." *Sensors and Actuators A: Physical* 77, no. 3 (November 1999): 237-244.

Outline

- Etching
- Wafer bonding
- Surface micromachining
- Process integration

Concerns in designing a process and mask set

- We know that we have to obey the laws of physics and the vendor's constraints when designing a process flow
- It's easier to design a robust, effective process if you've designed your device well
  - Selecting your device architecture wisely – if you don't design an unbuildable structure, you won't have to build it
  - Designing the package and packaging process during the device design

One concern: accumulated topography

- Successive steps of lithography and etching or deposition create non-planar surface topography
- This can interfere with further fabrication:
  - Getting good coverage with photoresist
  - Depth of focus of lithographic tool
  - Wafer bonding
  - Stringers left over from etching
- Chemical mechanical polishing (CMP) can be used to remove or reduce unwanted topographic features
- Other techniques available for special cases

Chemical Mechanical Polishing (CMP)

- Often used to planarize interlayer dielectric insulators
- Typical surface roughness less than of 1 nm (but waviness can be much bigger)
- Combination of mechanical polishing and chemical etching
- Using an abrasive slurry dispersed in an alkaline solution
- High, narrow features polish faster than low, uniform features

Stringers

- **Stringers form when a conformal film that covers topographic features is etched directionally, e.g. with RIE or dilute plasma**

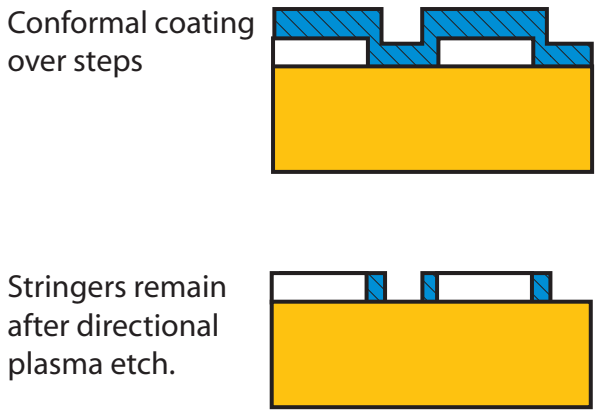


Image by MIT OpenCourseWare.
Adapted from Figure 3.34 in: Senturia, Stephen D. *Microsystem Design*. Boston, MA: Kluwer Academic Publishers, 2001, p. 74. ISBN: 9780792372462.

A Bad Stringer Location

- The material in the cusp is almost impossible to remove by etching
- Using a thicker white layer and polishing it back with CMP cures the stringer problem (so part of the cure is “don’t let it happen in the first place”… a good lesson to remember)

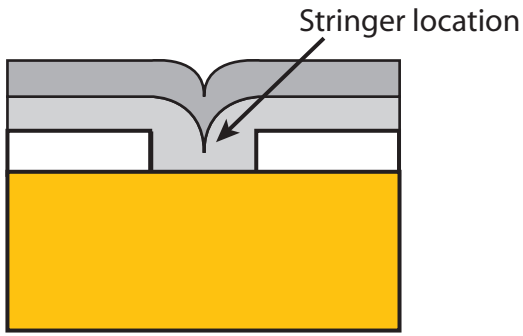


Image by MIT OpenCourseWare.

Adapted from Figure 3.35 in: Senturia, Stephen D. *Microsystem Design*. Boston, MA: Kluwer Academic Publishers, 2001, p. 75. ISBN: 9780792372462.

System partitioning

- You know that the overall system requires a set of functionalities. How many of them should you put on the MEMS chip? This will govern your fab process!
- Prime example: electronics
  - If you have a tiny signal that you can't detect without amplifying it as soon as it's produced, then you need at least first stage amplifying electronics
  - If on-chip electronics are not functionally required, you must choose whether it will save you money (fewer chips to make and package together) or cost you money (more ways to ruin your MEMS chip in the fab, and fewer process options) to include electronics on chip
- Some commercially successful devices are made with on-chip electronics
- More commonly, they are not

Die separation

- Usually you use single MEMS chips, rather than whole wafers
- When and how to cut the chips apart?
- If you're going to slice them apart with a (very ungentle) die saw, you must identify where in the process you will do it without breaking your structures
- One alternate approach: include etch features on your mask that will separate the dies most of the way so they snap apart at the end
- Either way, must think about this when creating your process flow

Design MEMS device and package together!

- You can't make the microfabricated part without photomasks
- The photomasks include interfaces to package:
  - Electrical bond pads, access required for MEMS function
- Until you make the system partitioning decision, you don't know the bond-pad requirements.
- Until you design the package, you don't know what the constraints on the physical access will be
- Therefore, until you make the system partitioning decision and design the package, you can't make the masks!
- Second order package-device interactions:
  - High temperature packaging step can affect device: thermal stresses, outgassing, etc.

Process design philosophy

- People publish their fab accomplishments
- Students read the papers and take home the wrong message
  - "They published X. X must be straightforward, and my process can probably count on accomplishing even a little more than X."
  - "W, X, Y, and Z have all been demonstrated. I can't count on doing any better than W, X, Y, and Z, but I'm sure I can accomplish all of them simultaneously."
- Some advice:
  - Don't design your processes on the hairy edge of impossibility.
  - Including a very difficult process may be unavoidable, but a) don't include a lot of them and b) be prepared to put a lot of work into making that process robust.
  - On the design projects, we will know if your process is too ambitious. In your thesis or in your job, Mother Nature will know if your process is too ambitious.