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6.776
High Speed Communication Circuits
Lecture 7
High Freqeuncy, Broadband Amplifiers

Massachusetts Institute of Technology

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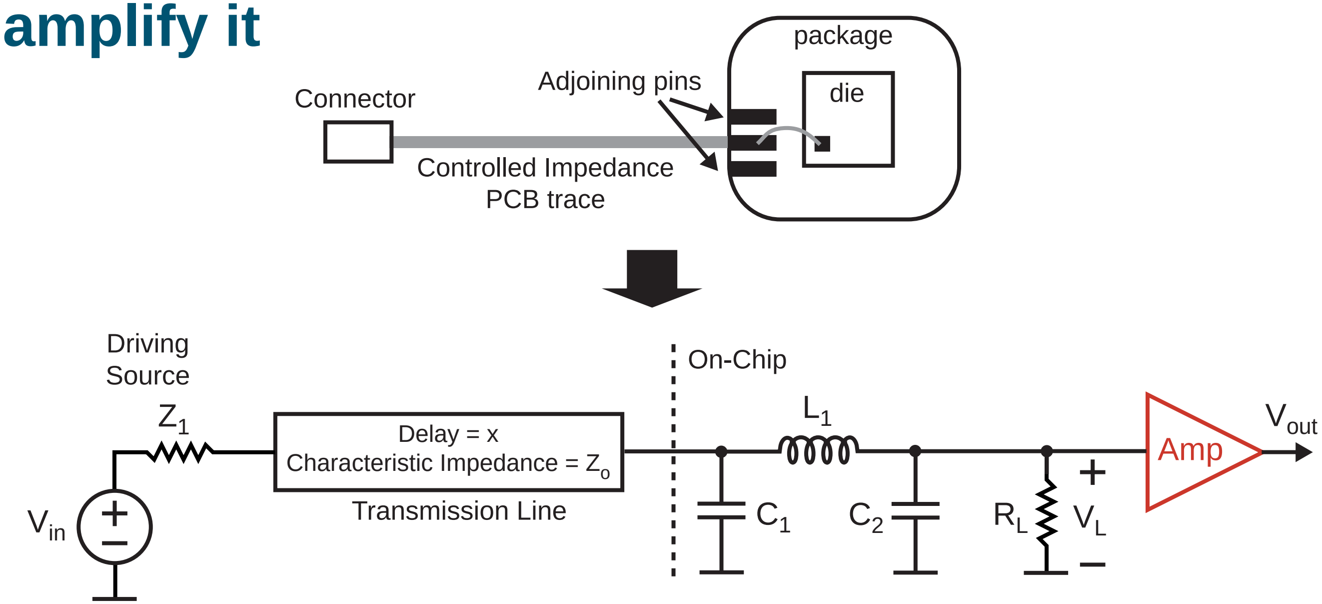
High Frequency, Broadband Amplifiers

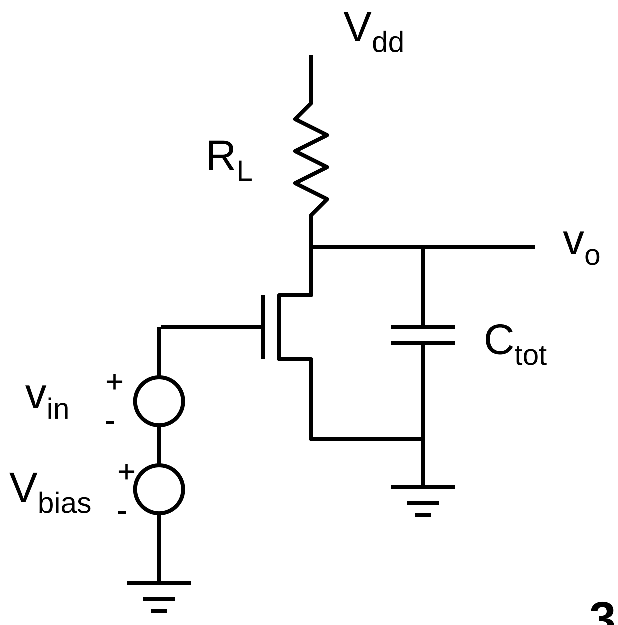
- The first thing that you typically do to the input signal is amplify it



- Function
  - Boosts signal levels to acceptable values
  - Provides reverse isolation
- Key performance parameters
  - Gain, bandwidth, noise, linearity

Gain-bandwidth Trade-off

- **Common-source amplifier example**



C_{tot}: total capacitance at output node

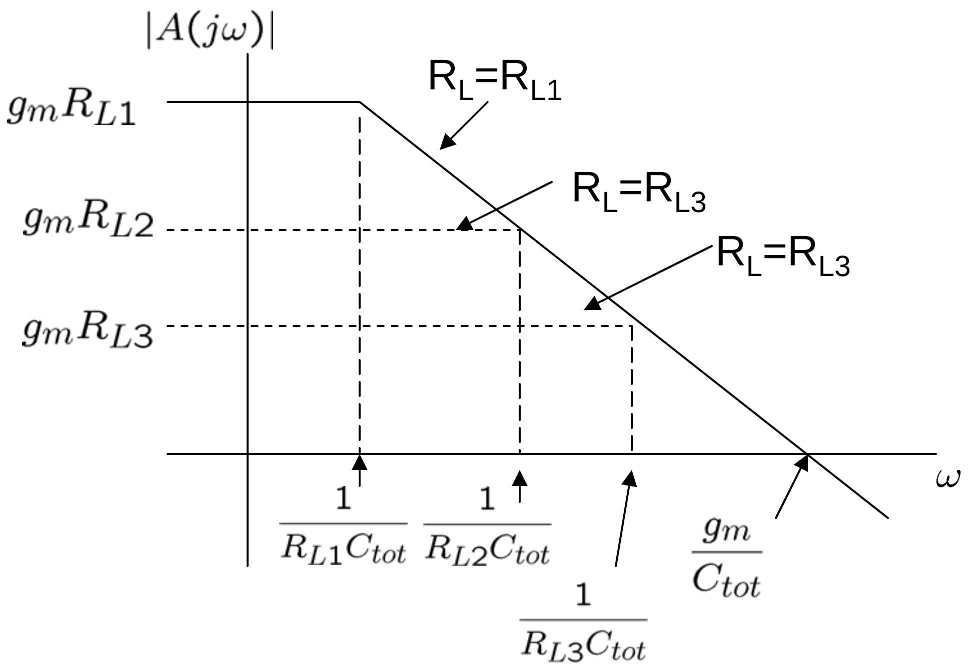
DC gain $A = g_m R_L$

3 dBbandwidth $\omega_h = \frac{1}{R_L C_{tot}}$

Gain-bandwidth $GB = \frac{g_m}{C_{tot}}$

Gain-bandwidth Trade-off

- **Common-source amplifier example**



- **Given the 'origin pole' g_m/C_{tot}, higher bandwidth is achieved only at the expense of gain**
- **The origin pole g_m/C_{tot} must be improved for better GB**

Gain-bandwidth Improvement

- **How do we improve g_m/C_{tot}?**
- **Assume that amplifier is loaded by an identical amplifier and fixed wiring capacitance is negligible**
- **Since** $g_m = \mu_n C_{ox} \frac{W}{L}(V_{GS} - V_T)$ **and** $C_{tot} \propto W$

$$\frac{g_m}{C_{tot}} \propto \frac{V_{GS} - V_T}{L}$$

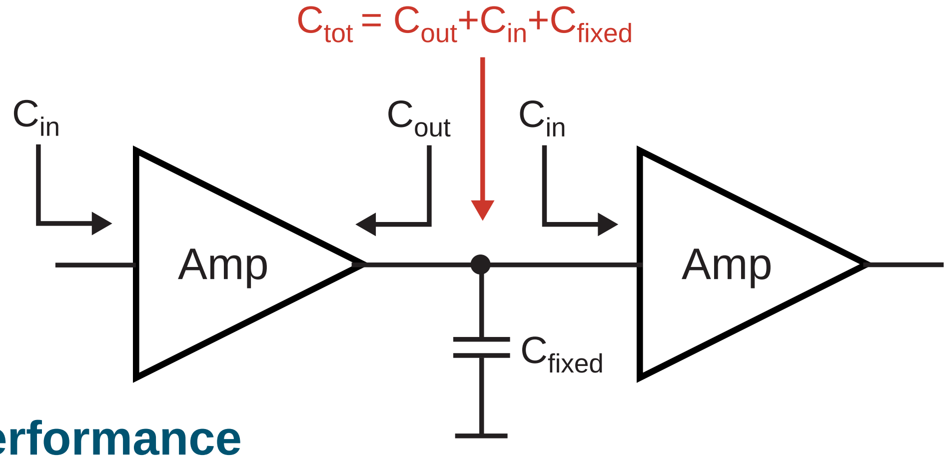
- **To achieve maximum GB in a given technology, use minimum gate length, bias the transistor at maximum** $V_{GS} - V_T$
- **When velocity saturation is reached, higher** $V_{GS} - V_T$ **does not give higher g_m**
- **In case fixed wiring capacitance is large, power consumption must be also considered**

Gain-bandwidth Observations

- Constant gain-bandwidth is simply the result of single-pole role off – it's *not* fundamental!
- It implies a single-pole frequency response may not be the best for obtaining gain and bandwidth simultaneously
- Single-pole role off is necessary for some circuits, e.g. for stability, but not for broad-band amplifiers

Assumptions (for now) for Bandwidth Analysis

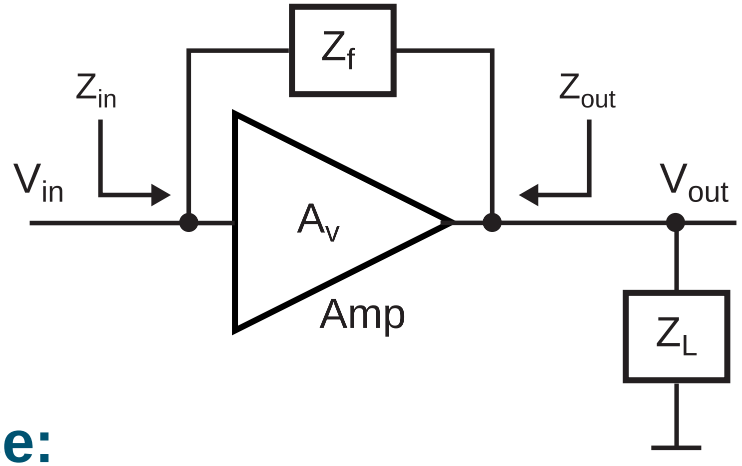
- **Assume for now that amplifier is loaded by an identical amplifier and by fixed wiring capacitance**
- **Assume amplifier is driven by an ideal voltage source for now**



- **Intrinsic performance**
  - **Defined as the bandwidth achieved for a given gain when C_{fixed} is negligible**
  - **Amplifier approaches intrinsic performance as its device sizes (and current) are increased**
- **In practice, point of diminishing return for bandwidth vs. size (and power) of amplifier is roughly where $C_{in}+C_{out} = C_{fixed}$**

The Miller Effect

- **Concerns impedances that connect from input to output of an amplifier**



- **Input impedance:**

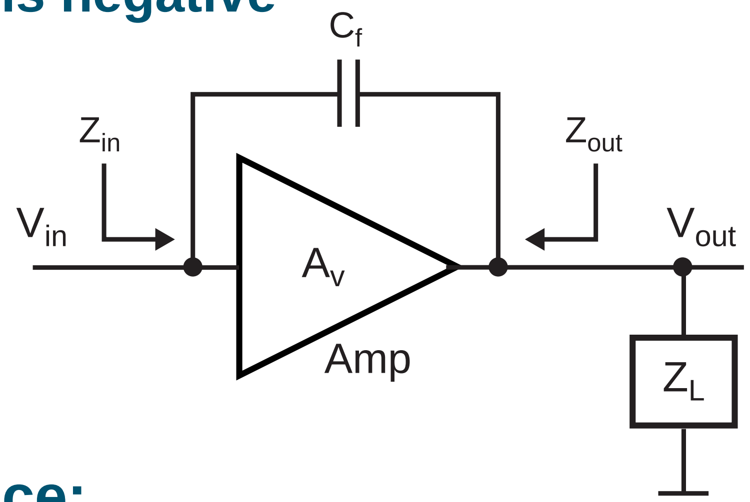
$$Z_{in} = \frac{V_{in}}{(V_{in} - V_{out})/Z_f} = \frac{Z_f}{1 - A_v}$$

- **Output impedance:**

$$Z_{out} = \frac{V_{out}}{(V_{out} - V_{in})/Z_f} = \frac{Z_f}{1 - 1/A_v} \approx Z_f \text{ for } |A_v| \gg 1$$

Example: Miller Capacitance

- Consider C_{gd} in the MOS device as C_f
  - Assume gain is negative

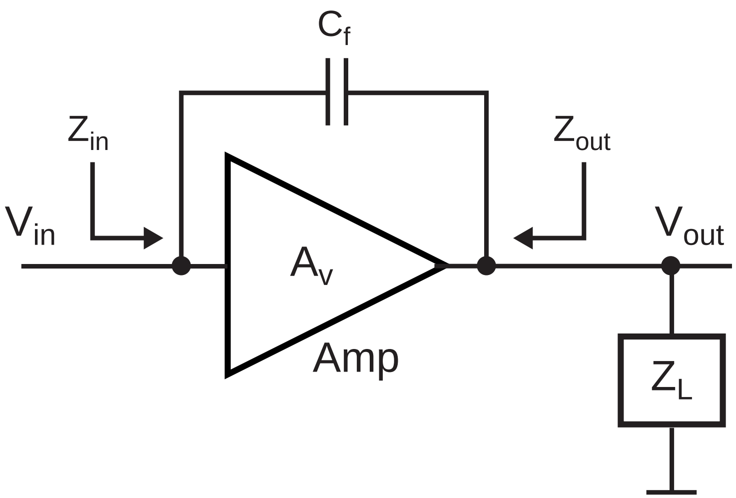


- Input capacitance:

$$Z_{in} = \frac{1/(sC_f)}{1+|A_v|} = \frac{1}{sC_f(1+|A_v|)}$$

Looks like much larger capacitance by $|A_v|$

Example: Miller Capacitance



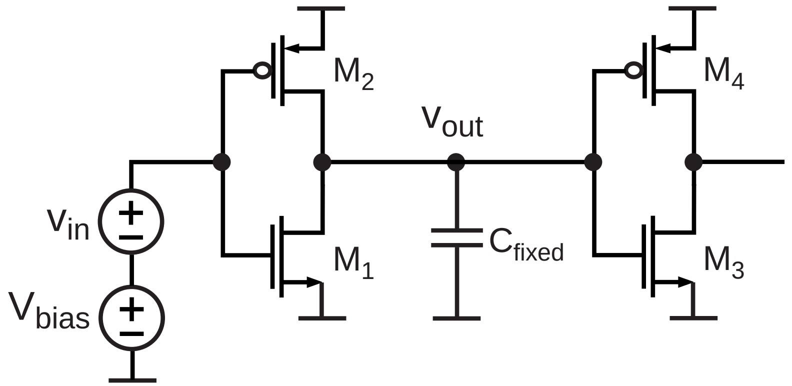
- **Output impedance:**

$$Z_{out} = \frac{1/(sC_f)}{1 + 1/|A_v|} = \frac{1}{sC_f(1 + 1/|A_v|)} \approx \frac{1}{sC_f}$$

This makes sense because the input of the amplifier is 'virtual ground' if gain is large

Amplifier Example – CMOS Inverter

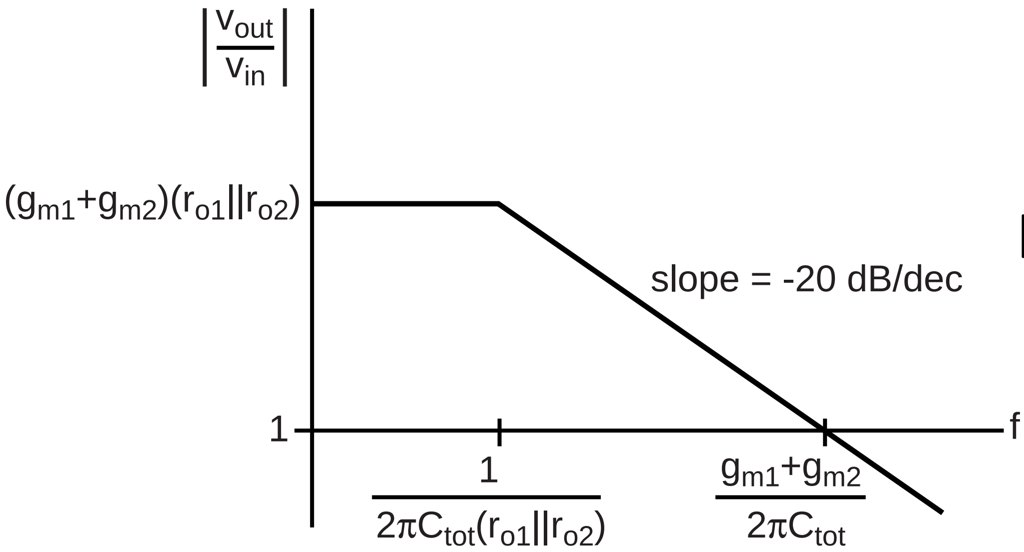
- **The Miller effect gives a quick way to estimate the bandwidth of an amplifer without solving node equations: intuition!**
- **Assume that we set V_{bias} the amplifier nominal output is such that NMOS and PMOS transistors are all in saturation**
  - **Note: this topology VERY sensitive to V_{bias} : some feedback biasing would be required (6.301)**



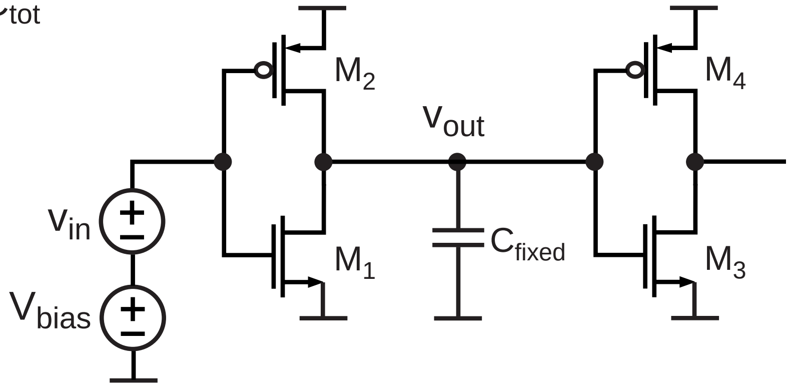
$$C_{tot} = C_{db1}+C_{db2} + C_{gs3}+C_{gs4} + K(C_{ov3}+C_{ov4}) + C_{fixed}$$

$(+C_{ov1}+C_{ov2})$ Miller multiplication factor

Transfer Function of CMOS Inverter



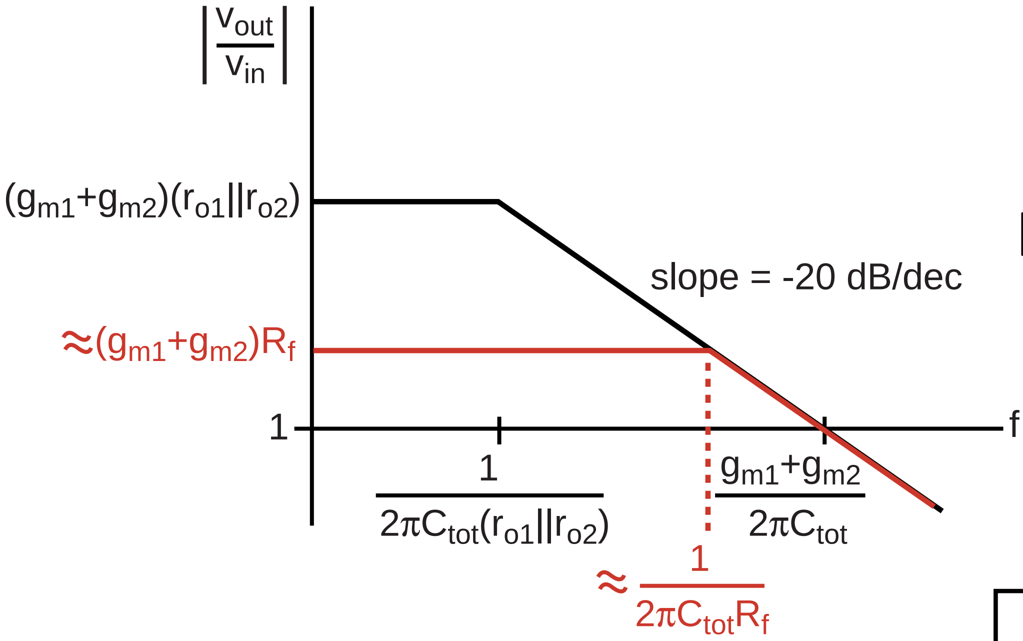
Low Bandwidth!



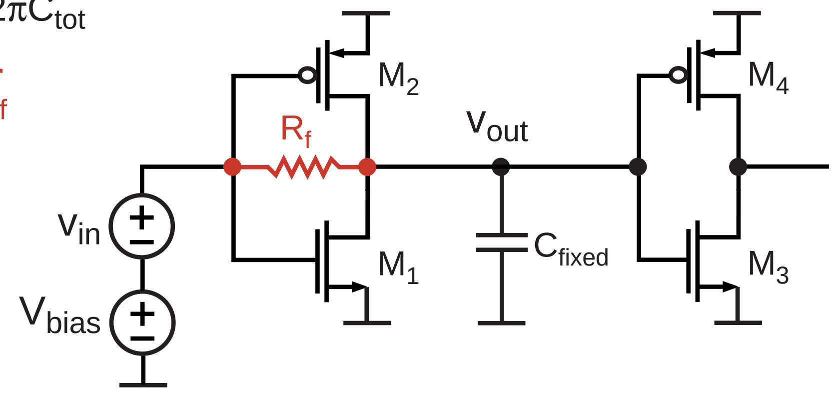
$C_{tot} = C_{db1}+C_{db2} + C_{gs3}+C_{gs4} + K(C_{ov3}+C_{ov4}) + C_{fixed}$

$(+C_{ov1}+C_{ov2})$ Miller multiplication factor

Add Resistive Feedback?



Bandwidth extended and less sensitivity to bias offset (does not improve GB, though)

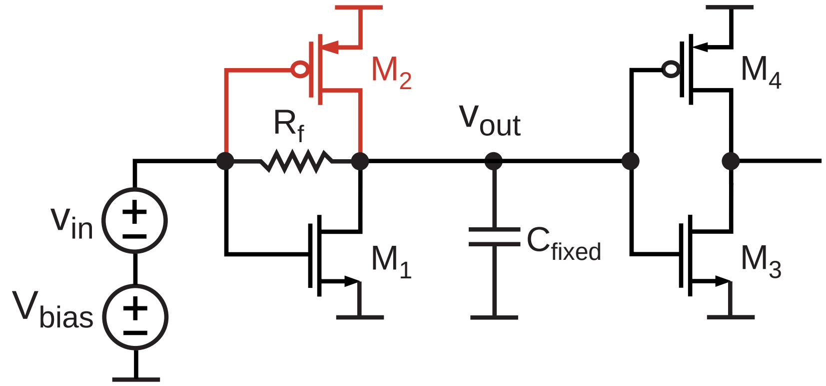


$$C_{tot} = C_{db1}+C_{db2} + C_{gs3}+C_{gs4} + K(C_{ov3}+C_{ov4}) + C_{Rf}/2 + C_{fixed}$$

$(+C_{ov1}+C_{ov2})$ — Miller multiplication factor

We Can Still Do Better

- We are fundamentally looking for high g_m to capacitance ratio to get the highest bandwidth
  - PMOS degrades this ratio
  - Gate bias voltage is constrained
- However, when C_{fixed} is dominant and power consumption is important, the PMOS increases g_m without additional power
- On the other hand, below velocity saturation, higher g_m can be achieved by biasing the gate of M_1 close to V_{dd} instead of using PMOS

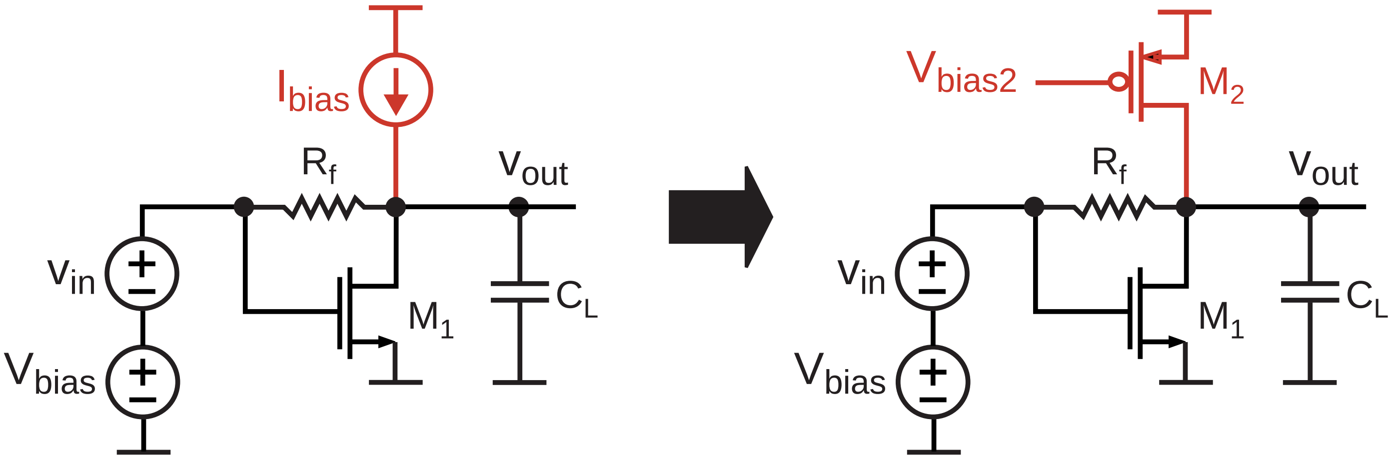


$$C_{tot} = C_{db1} + C_{db2} + C_{gs3} + C_{gs4} + K(C_{ov3} + C_{ov4}) + C_{Rf}/2 + C_{fixed}$$

$(+C_{ov1}+C_{ov2})$ ↑ (added to $C_{db1}+C_{db2}$)

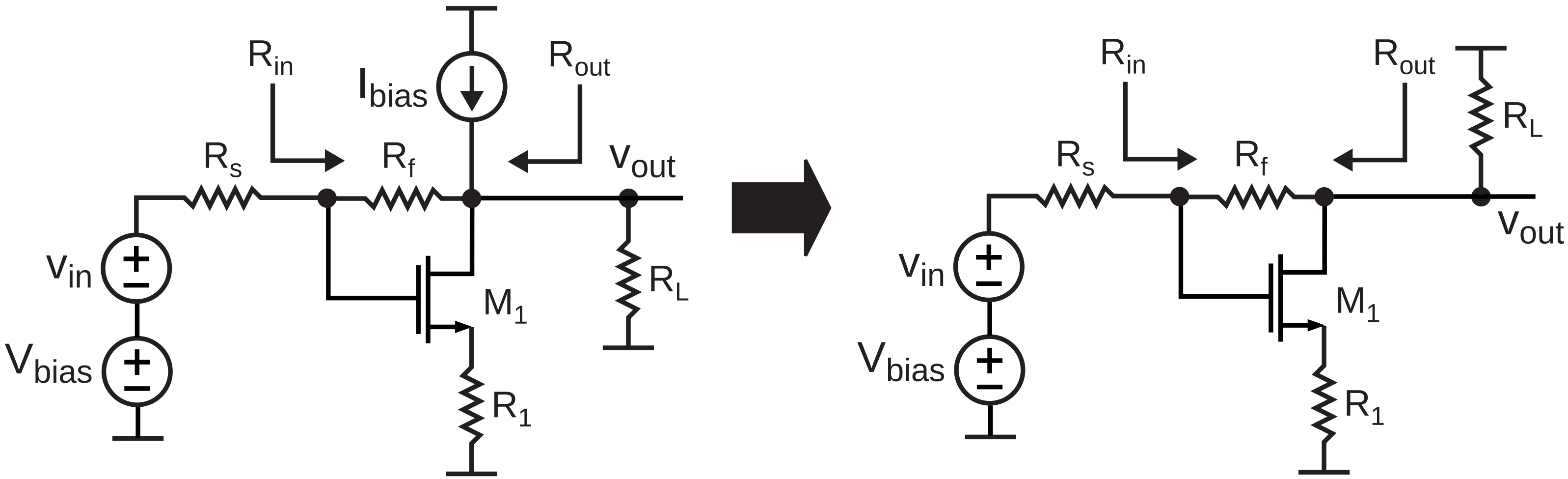
Miller multiplication factor ↑ (K)

Take PMOS Out of the Signal Path



- **Advantages**
  - **PMOS gate no longer loads the signal**
  - **NMOS device can be biased at a higher voltage (higher g_m up to velocity sat. limit)**
- **Issue**
  - **PMOS is not an efficient current provider (I_d/drain cap C_{gd}+C_{db})**
    - Drain cap close in value to C_{gs}
  - **Signal path is loaded by cap of R_f and drain cap of PMOS**

Shunt-Series Amplifier



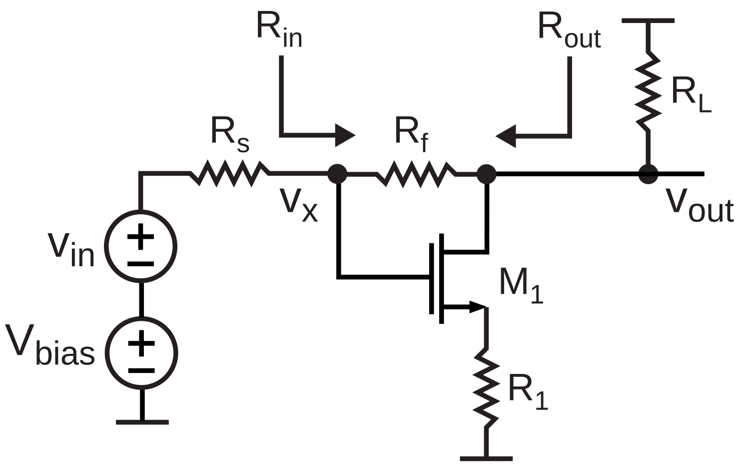
- **Use resistors to control the bias, gain, and input/output impedances**
  - **Improves accuracy over process and temp variations**
- **Issues**
  - **Degeneration of M_1 lowers slew rate for large signal applications (such as limit amps)**
  - **There are better high speed approaches – the advantage of this one is simply accuracy**

Shunt-Series Amplifier – Analysis Snapshot

- From Chapter 9 (8) of Tom Lee's book:
  - Gain

$$A_v = \frac{v_{out}}{v_{in}} = -\frac{R_L}{R_E}\left(\frac{R_f - R_E}{R_f + R_L}\right)$$

where: $R_E = 1/g_m + R_1$



Note: $A_v \approx -\frac{R_L}{R_1}$ for $R_f \gg R_L,\ R_f \gg R_E,\ R_1 \gg 1/g_m$

  - Input resistance

$$R_{in} = \frac{R_f}{1 - A_v} = \frac{R_E(R_f + R_L)}{R_E + R_L} \approx \frac{R_f}{1 + R_L/R_1}$$

for $R_f \gg R_L$, $R_1 \gg 1/g_m$

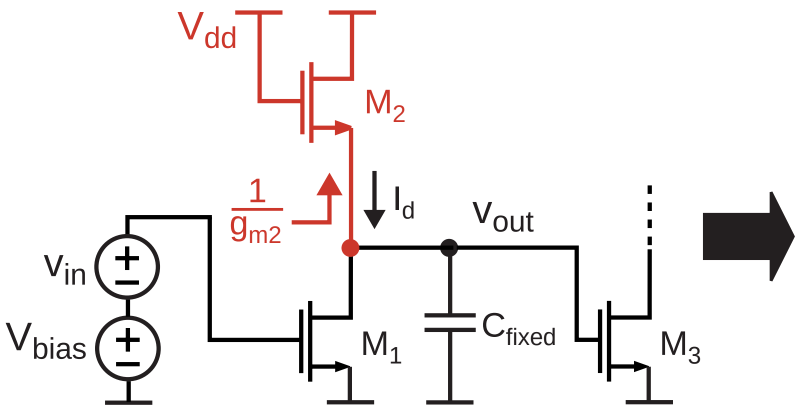
  - Output resistance

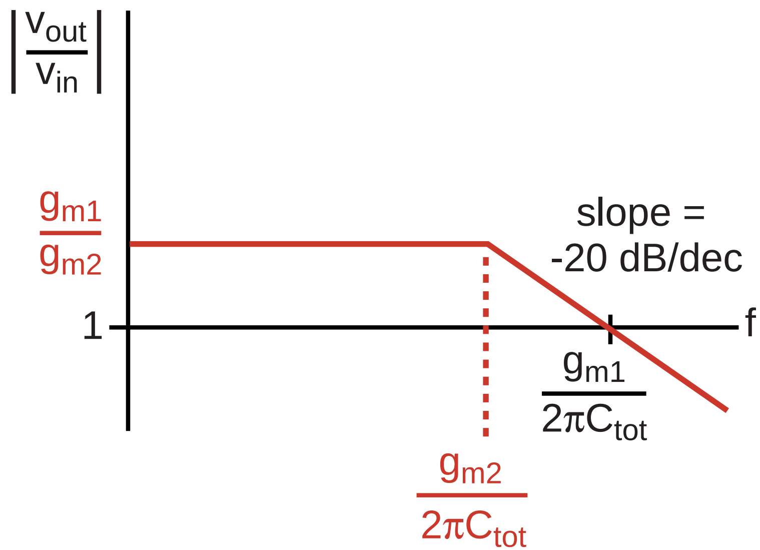
$$R_{out} = \frac{R_E(R_f + R_s)}{R_E + R_s} \approx \frac{R_f}{1 + R_s/R_1}$$

Same for $R_s = R_L$!

for $R_f \gg R_s,\ R_1 \gg 1/g_m$

NMOS Load Amplifier





$C_{tot} = C_{db1} + C_{sb2} + C_{gs2} + C_{gs3} + KC_{ov3} + C_{fixed}$

($+C_{ov1}$) — Miller multiplication factor

- **Gain set by the relative sizing of M_1 and M_2**

$$M_1: \; I_{d1} = (1/2)\mu_n C_{ox}(W_1/L_1)(V_{IN} - V_T)^2$$

$$M_2: \; I_{d2} = (1/2)\mu_n C_{ox}(W_2/L_2)(V_{dd} - V_{out} - V_T)^2$$

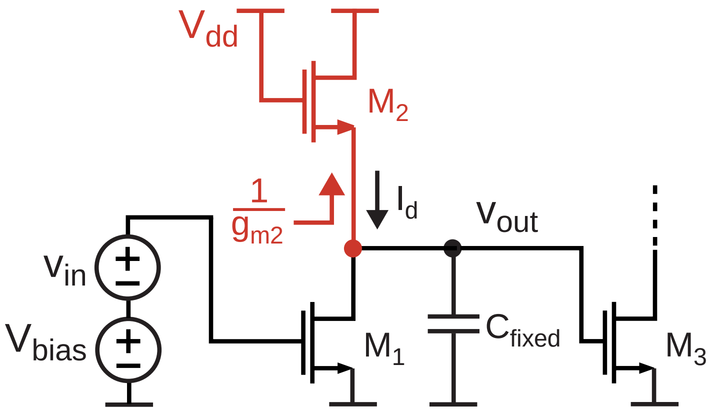
$$\Rightarrow I_{d1} = I_{d2}$$

$$\Rightarrow V_{out} = -AV_{IN} + V_{dd} + (A-1)V_T$$

$$(V_{IN} = V_{in} + V_{bias})$$

where $A = \sqrt{\dfrac{W_1/L_1}{W_2/L_2}}$

Design of NMOS Load Amplifier



$$C_{tot} = C_{db1} + C_{sb2} + C_{gs2} + C_{gs3} + KC_{ov3} + C_{fixed}$$

$(+C_{ov1})$ Miller multiplication factor

$$A = \sqrt{\frac{W_1/L_1}{W_2/L_2}}$$

- **Size transistors for gain and speed**
  - **Choose minimum L for maximum speed**
  - **Choose ratio of W_1 to W_2 to achieve appropriate gain**

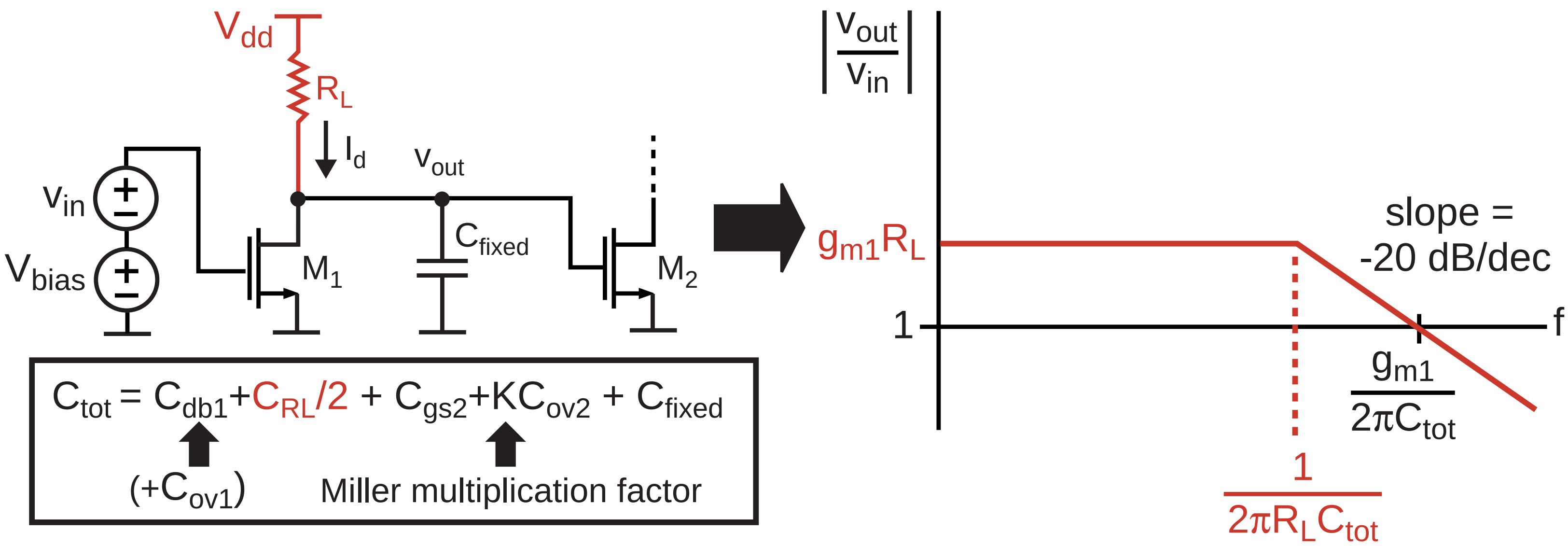
Advantage/Disadvantages of NMOS Load Amplifier

- **Gain is well controlled despite process variations**

- **NMOS is not a low parasitic load**
  - **C_{gs} of M2 loads the output**

- **Biasing Problem: V_T of M_2 lowers the gate bias voltage of the next stage (thus lowering its achievable f_t)**
  - **Severely hampers performance when amplifier is cascaded**
  - **One paper addressed this issue by increasing V_{dd} of NMOS load (see Sackinger et. al., "A 3-GHz 32-dB CMOS Limiting Amplifier for SONET OC-48 receivers", JSSC, Dec 2000)**

Resistor Loaded Amplifier (Unsilicided Poly)



$C_{tot} = C_{db1} + C_{RL}/2 + C_{gs2} + KC_{ov2} + C_{fixed}$

$(+C_{ov1})$ — Miller multiplication factor

- **This is the fastest non-enhanced amplifier topology**
  - **Unsilicided poly is a low parasitic load (i..e, has a good current to capacitance ratio)**
  - **Output can go near V_{dd}**
    - Allows following stage to achieve high f_t , but at the cost of gain (max gain $\propto V_{R_L}$)
  - **Linear settling behavior (in contrast to NMOS load)**

Gain Limitations in Resistor Loaded Amplifier

$$g_m = \frac{dI_d}{dV_{gs}} = \frac{2I_d}{V_{GS} - V_T}$$

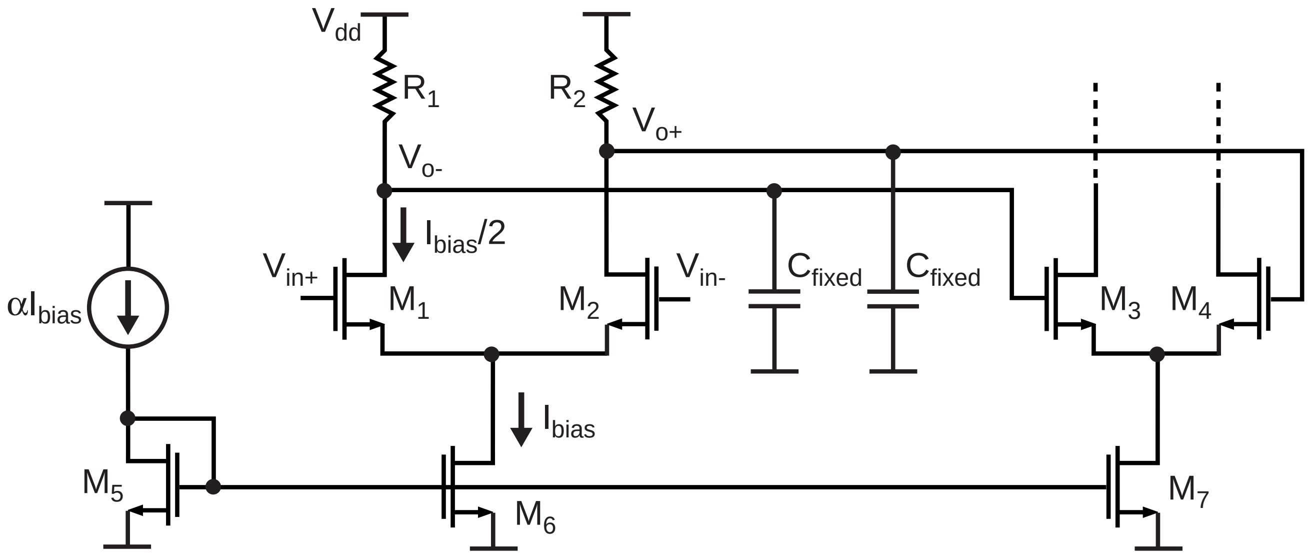
$$A = g_m R_L = \frac{2I_d R_L}{V_{GS} - V_T} = \frac{2V_{R_L}}{V_{GS} - V_T}$$

$$A_{MAX} = \frac{2V_{dd}}{V_{GS} - V_T}$$

- **Want high $V_{GS} - V_T$ for high bandwidth, but this reduces gain. With low V_{dd} gain is very limited.**

Implementation of Resistor Loaded Amplifier

- **Typically implement using differential pairs**



- **Benefits**
  - **Bias stability without feedback**
  - **Common-mode rejection**
- **Negative**
  - **More power than single-ended version**

Open-Circuit Time Constants

- **The Miller capacitance analysis is a reasonably good method, but is somewhat limited in applicable topologies**
- **the OCT method is more general and often gives more insights**
- **Systematic, intuitive method to determine bandwidth of amplifiers**
- **Often gives fairly accurate estimates of bandwidth if there is a dominant pole**
- **Points to the bandwidth *bottleneck*: this is the *real* value of the OCT method!**
- **Limitation: fails in RF circuits with zero enhancements or inductors**
- **In typical broadband amplifiers, the OCT estimate is *too pessimistic* due to multiple poles at around similar frequencies**

Open Circuit Time Constant Method

Assumptions: **No zero near or ω_h**
Zero well below wh is handled by treating corresponding capacitor as sort circuit
Negative real poles only (complex conjugate poles with low Q reduces accuracy of estimation only moderately)
No inductors

$$A(s) = \frac{V_o}{V_i} = \frac{a_0}{(1+\tau_1 s)(1+\tau_2 s)\cdots(1+\tau_n s)}$$

$$= \frac{a_0}{1+(\tau_1+\tau_2+\cdots+\tau_n)s\cdots\tau_1\tau_2\cdots\tau_n s^n}$$

If we ignore the higher order terms

$$\omega_h = 2\pi f_h \approx \frac{1}{\tau_1+\tau_2+\cdots+\tau_n} = \frac{1}{\sum_{i=1}^{n}\tau_i}$$

OCT Method, Continued

It can be shown

$$\sum_{i=1}^{n} \tau_i = \sum_{j=1}^{n} \tau_{jo}$$

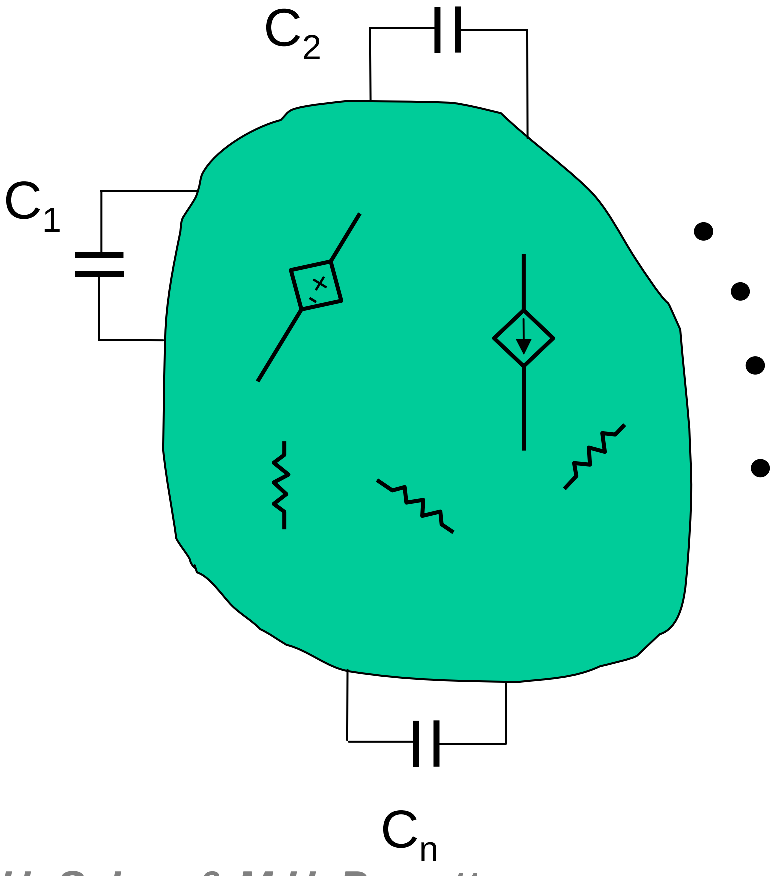
Thus $\omega_h \approx \frac{1}{\sum_{j=1}^{n} \tau_{jo}}$

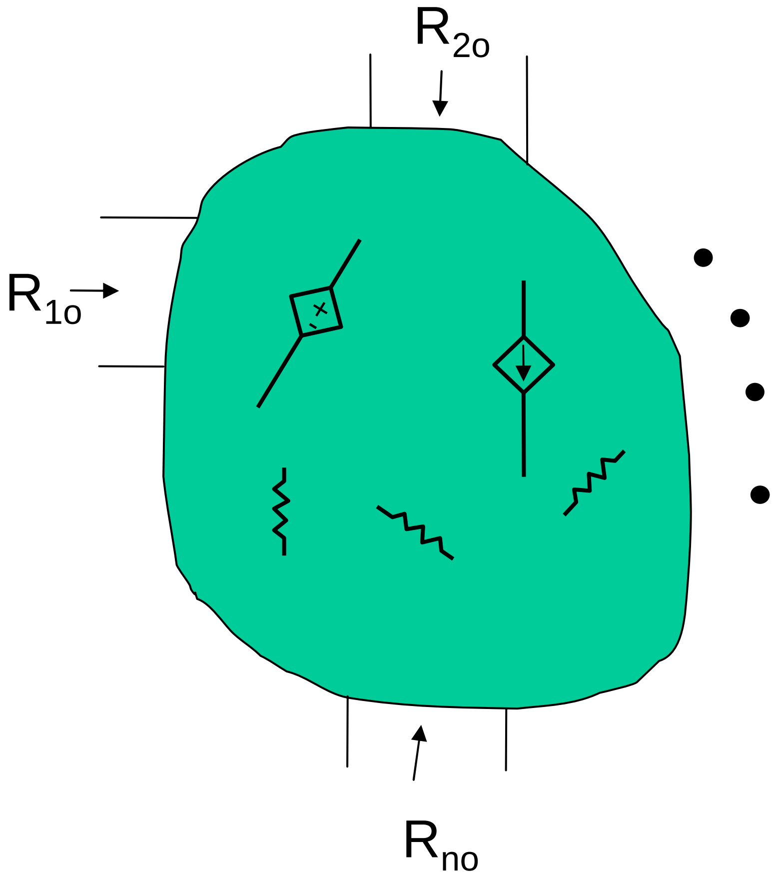
where $\tau_{jo} = R_{jo} C_j$ **:open-circuit time constants**

The open-circuit time constants can be found without node equations, often by inspection

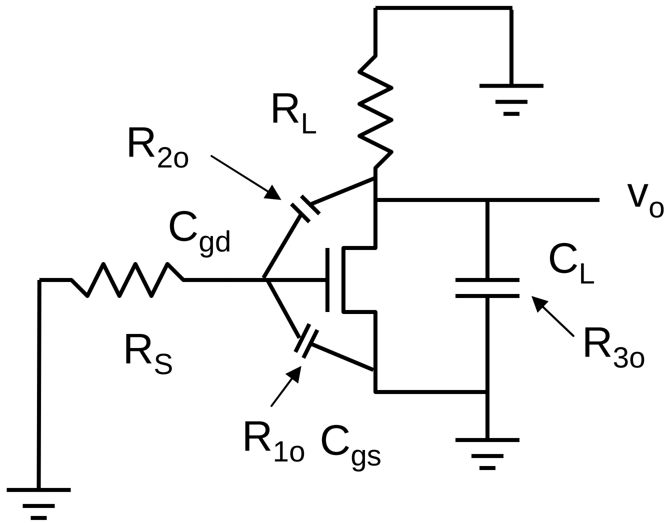
OCR Calculation

Let's consider an arbitrary circuit with resistors, dependent sources, and n capacitors (no inductors!). Redraw the circuit to pull capacitors out around the perimeter.





OCT's for CS Amplifier



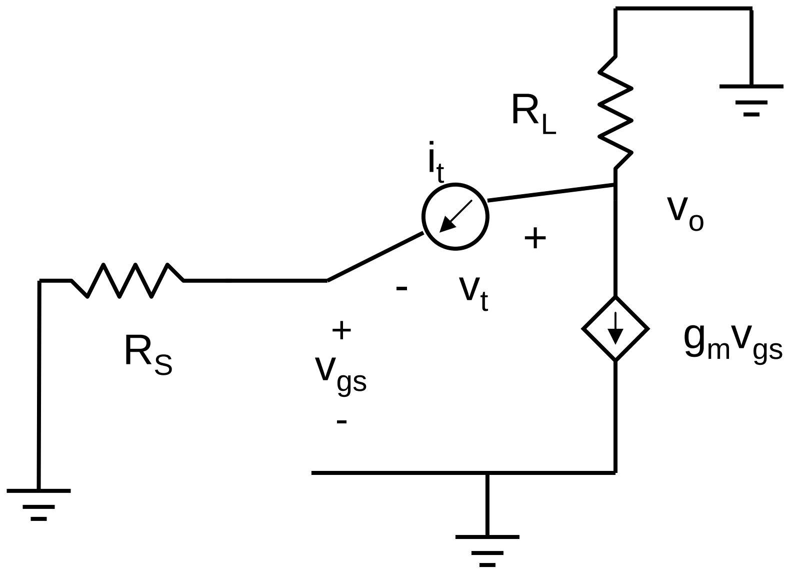
By inspection:

$$R_{1o} = R_S, \;\; \tau_{1o} = R_S C_{gs}$$

$$R_{3o} = R_L, \;\; \tau_{3o} = R_L C_L$$

It takes some work to figure R_{2o}

OCT's for CS Amplifier



$$v_{gs} = i_t R_S$$

$$-v_o = (i_t + g_m v_{gs})R_L = i_t(1 + g_m R_S)R_L$$

$$v_t = v_{gs} - v_o = i_t(1 + \frac{R_S}{R_L} + g_m R_S)R_L$$

$$R_{2o} = \frac{v_t}{i_t} = (1 + \frac{R_S}{R_L} + g_m R_S)R_L$$

$$\tau_{2o} = C_{gd}(1 + \frac{R_S}{R_L} + g_m R_S)R_L$$

OCT's for CS Amplifier

$$R_{1o} = R_S, \;\; \tau_{1o} = R_S C_{gs}$$

$$R_{3o} = R_L, \;\; \tau_{3o} = R_L C_L$$

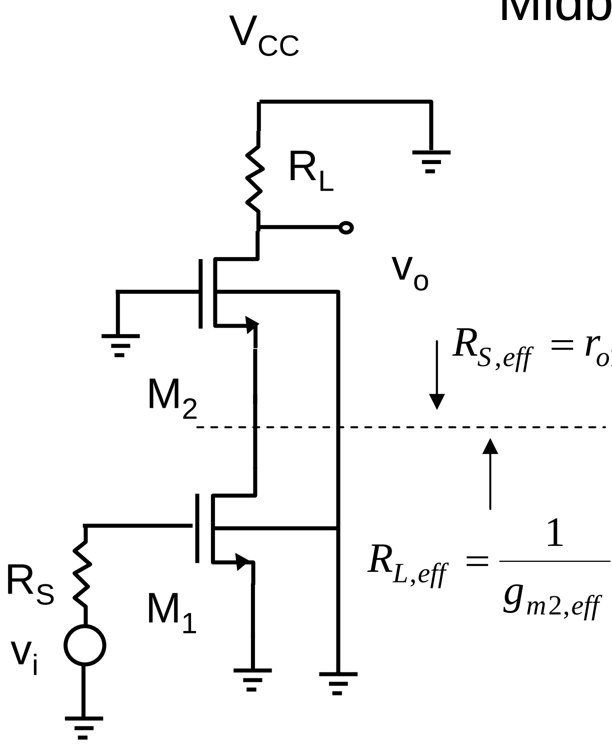
$$R_{2o} = \frac{v_t}{i_t} = (1 + \frac{R_S}{R_L} + g_m R_S) R_L$$

$$\tau_{2o} = C_{gd}(1 + \frac{R_S}{R_L} + g_m R_S) R_L = C_{gd}(1 + \frac{R_L}{R_S} + g_m R_L) R_S$$

- **If R_S=0, then τ_{1o}=0, τ_{2o}=$C_{gd}R_L$, and τ_{3o}=$C_L R_L$ so R_L determines the bandwidth**
- **Having individual OCT values identifies the bandwidth bottleneck and suggests a game plan**
- **Note:for cascased amplifiers, C_L does not include Miller cap of the next stage. Instead, τ_{2o} corresponding to the next stage Miller cap is separately calculated**

Cascode to Improve Bandwidth

Midband gain: by inspection $a_v = -g_{m1}R_L$



$$R_{S,eff} = r_{o1}$$

$$R_{L,eff} = \frac{1}{g_{m2,eff}} = \frac{1}{g_{m2} + g_{mb2}}$$

$$R_{1o} = R_S$$

$$R_{2o} = R_{1o}\left(1 + g_{m1}R_{L,eff} + \frac{R_{L,eff}}{R_S}\right)$$

$$= R_S + (1 + g_{m1}R_S)R_{L,eff}$$

$$= R_S + \frac{1 + g_{m1}R_S}{g_{m2} + g_{mb2}}$$

$$R_{3o} \approx R_{S,eff} \,\|\, \frac{1}{g_{m2,eff}} \approx \frac{1}{g_{m2} + g_{mb2}}$$

$$R_{4o} = \cancel{r_o}\left(1 + \frac{R_L}{\frac{1}{g_{m,eff}} + R_{S,eff}}\right) + R_L \approx R_L$$

Cascode

- **Improves bandwidth in a single-stage amplifier**

- **Problem in cascading:**
  - **Bias point: Reduces ω_t of the next stage. PMOS SF is a possibility but low g_m/C ratio is a drawback.**