MIT OPENCOURSEWARE
MASSACHUSETTS INSTITUTE OF TECHNOLOGY

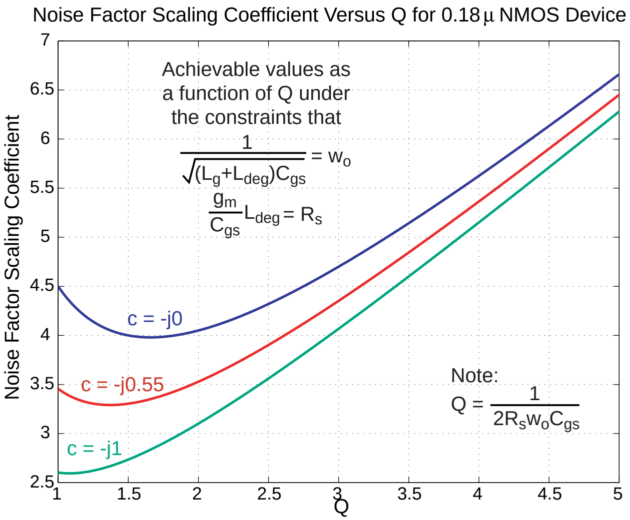
6.776
High Speed Communication Circuits and Systems
Lecture 13
LNA Design Examples and Recent Techniques

Massachusetts Institute of Technology

March 17, 2005

LNA Design Example

- **In our previous design example, we picked the Q for the minimum possible noise factor: Q=1.4**
- **We (arbitrarily) chose V_{gs}=1V**



The design yields

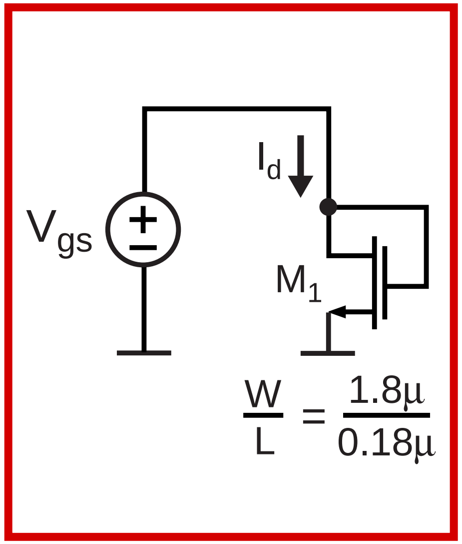
$$\text{Noise Factor} = 1.12 \text{ and Noise Figure} = 0.49dB$$

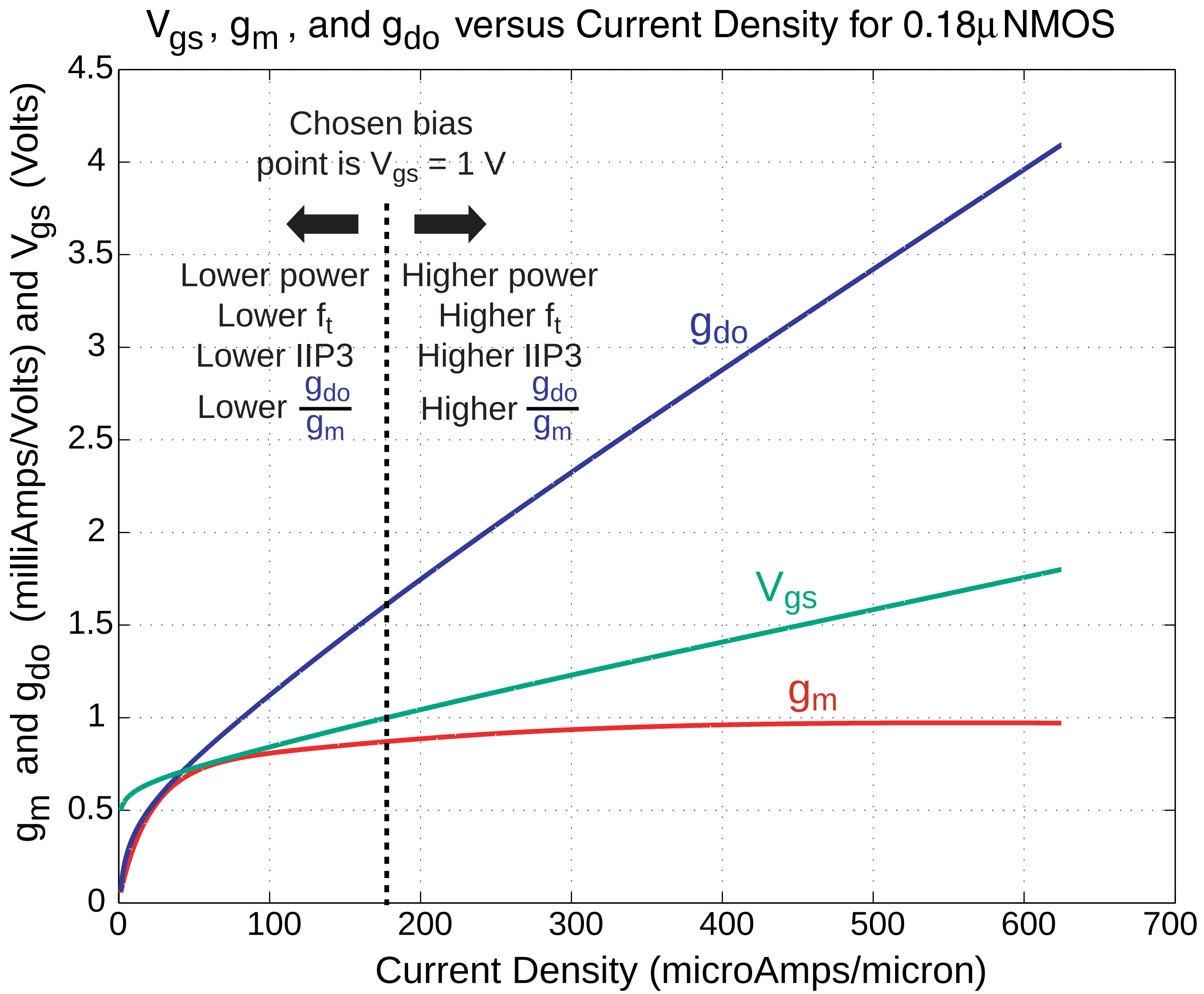
And requires

$$Cgs = 631fF, L_{deg} = 0.17nH, L_g = 12.2nH$$

$$W = 392\mu, I_{bias} = 69mA$$

Bias Point (V_{gs} = 1V)





- **Problem: the device is in velocity saturation**

We Have Two "Handles" to Lower Power Dissipation

- **Key formulas** $I_{bias} = I_{den} W$

$$F = 1 + \left(\frac{w_o}{w_t}\right)\gamma\left(\frac{g_{do}}{g_m}\right)\frac{1}{2Q}\left(1 - 2|c|\chi_d + (4Q^2+1)\chi_d^2\right)$$

- **Lower current density, I_{den}**
  - **Benefits**

$$\Rightarrow \text{ lower power, lower } \frac{g_{do}}{g_m} \text{ ratio}$$

  - **Negatives**

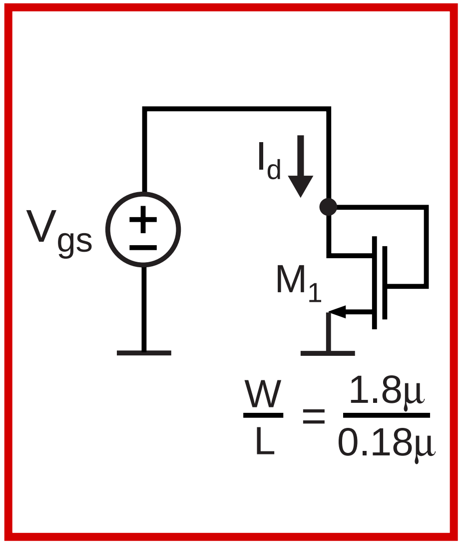
$$\Rightarrow \text{ lower IIP3, lower } f_t$$

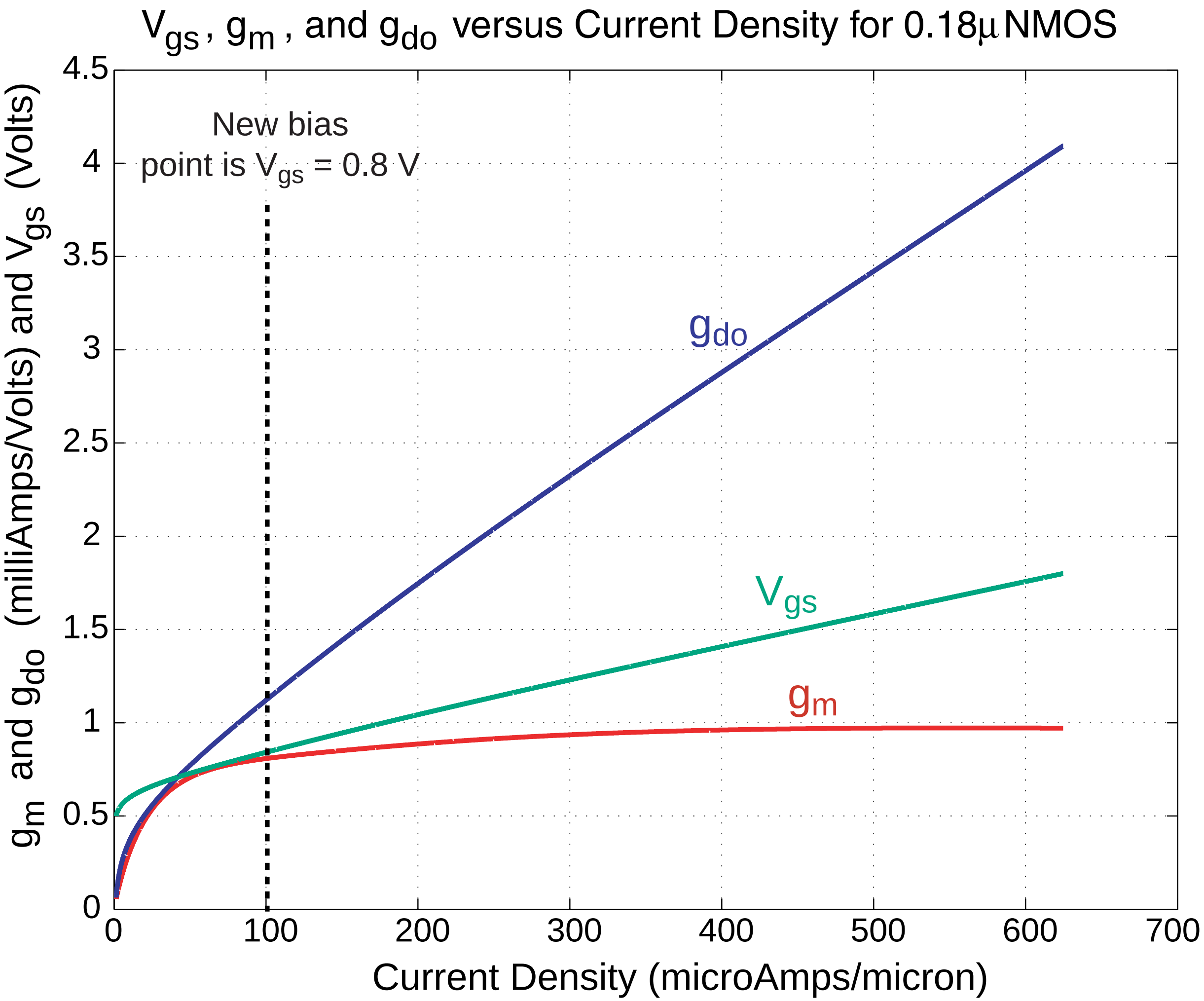
- **Lower W**
  - **Benefit: lower power**
  - **Negatives**

$$\Rightarrow \text{ lower } C_{gs} = \frac{2}{3}WLC_{ox} \Rightarrow \text{ higher } Q = \frac{1}{w_o C_{gs} 2R_s}$$

$$\Rightarrow \text{ higher } F \quad \text{(and higher inductor values)}$$

First Step in Redesign – Lower Current Density, I_{den}





- **Need to verify that IIP3 still OK (once we know Q)**

Recalculate Process Parameters

- **Assume that the only thing that changes is g_m/g_{do} and f_t**
  - **From previous graph (I_{den} = 100 μ A/μ m)**

$$\frac{g_m}{g_{do}} \approx \frac{.78}{1.15} \approx 0.68 \Rightarrow \chi_d = \frac{g_m}{g_{do}}\sqrt{\frac{\delta}{5\gamma}} = 0.63\sqrt{\frac{2}{5}} \approx 0.43$$

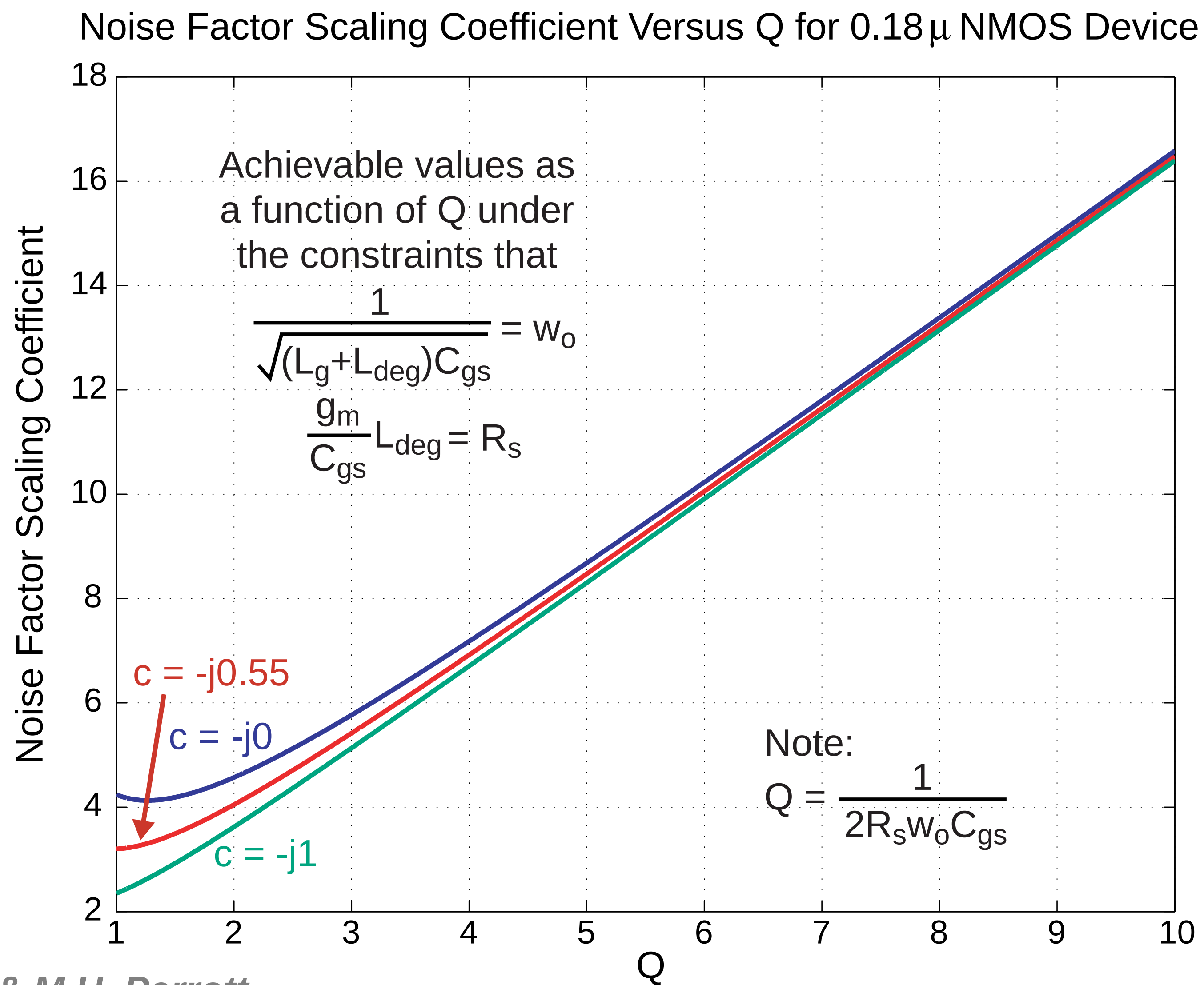
$$w_t \approx \frac{g_m}{C_{gs}} \approx \frac{0.78mS}{2.9fF} = (2\pi)42.8GHz$$

- **We now need to replot the Noise Factor scaling coefficient**
  - **Also plot over a wider range of Q**

$$F = 1 + \left(\frac{w_o}{w_t}\right)\underbrace{\gamma\left(\frac{g_{do}}{g_m}\right)\frac{1}{2Q}\left(1 - 2|c|\chi_d + (4Q^2+1)\chi_d^2\right)}_{\text{Noise Factor scaling coefficient}}$$

Noise Factor scaling coefficient

Update Plot of Noise Factor Scaling Coefficient



Second Step in Redesign – Lower W (or Raise Q)

- **Recall**

$$C_{gs} = \frac{2}{3} W L C_{ox}, \quad Q = \frac{1}{w_o C_{gs} 2R_s}$$

- **I_{bias} can be related to Q as**

$$I_{bias} = I_{den} W = I_{den} \frac{3}{2LC_{ox}} C_{gs} = I_{den} \frac{3}{2LC_{ox}} \frac{1}{w_o 2R_s Q}$$

$$\Rightarrow \boxed{I_{bias} \propto \frac{1}{Q}}$$

- **We previously chose Q = 1.4, let's now choose Q = 6**
  - **This alone cuts power dissipation by more than a factor of 4. Combined with lower I_{den}, almost a factor of 8 reduction in power**
  - **New value of W :** $\Rightarrow W = 392\mu \cdot \frac{1.4}{6} \approx \boxed{91\mu m}$

Power Dissipation and Noise Figure of New Design

- **Power dissipation**

$$I_{bias} = I_{den}W = (100\mu A/\mu m)(91\mu m) = \boxed{9.1mA}$$

  - **At 1.8 V supply**

$$\Rightarrow \quad \text{Power} = (9.1mA)(1.8V) = \boxed{16.4mW}$$

- **Noise Figure**
  - **f_t previously calculated, get scaling coeff. from plot**

$$\frac{w_o}{w_t} = \frac{2\pi 1.8e9}{2\pi 42.8e9} \approx \frac{1}{23.8}, \quad \text{scaling coeff.} \approx 10$$

$$\Rightarrow \quad \text{Noise Factor} \approx 1 + \frac{1}{23.8}10 \approx 1.42$$

$$\Rightarrow \quad \text{Noise Figure} = 10\log(1.42) \approx \boxed{1.52\ dB}$$

Updated Component Values

- Assume R_s = 50 Ohms, Q = 6, f_o = 1.8 GHz, f_t = 42.8 GHz
  - C_{gs} calculated as

$$Q = \frac{1}{2R_s w_o C_{gs}}$$

$$\Rightarrow \; C_{gs} = \frac{1}{2R_s w_o Q} = \frac{1}{2(50)2\pi 1.8e9(6)} \approx \boxed{147fF}$$

  - L_{deg} calculated as

$$\frac{g_m}{C_{gs}} L_{deg} = R_s \;\; \Rightarrow \;\; L_{deg} = \frac{R_s}{w_t} = \frac{50}{2\pi 42.8e9} = \boxed{0.19nH}$$

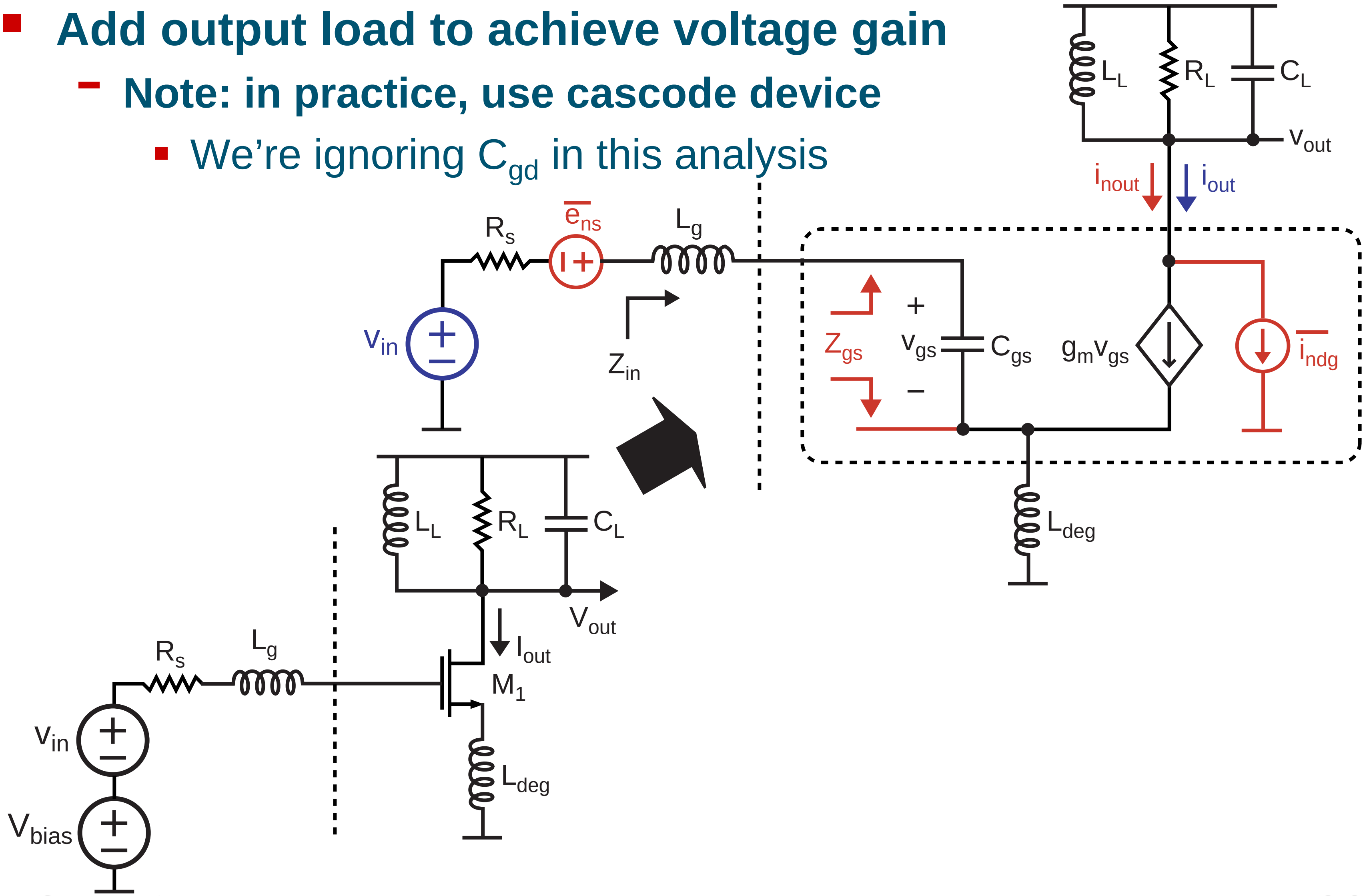
  - L_g calculated as

$$\frac{1}{\sqrt{(L_g + L_{deg})C_{gs}}} = w_o \;\Rightarrow\; L_g = \frac{1}{w_o^2 C_{gs}} - L_{deg}$$

$$\Rightarrow \; L_g = \frac{1}{(2\pi 1.8e9)^2 147e\text{-}15} - 0.19e\text{-}9 = \boxed{53nH}$$

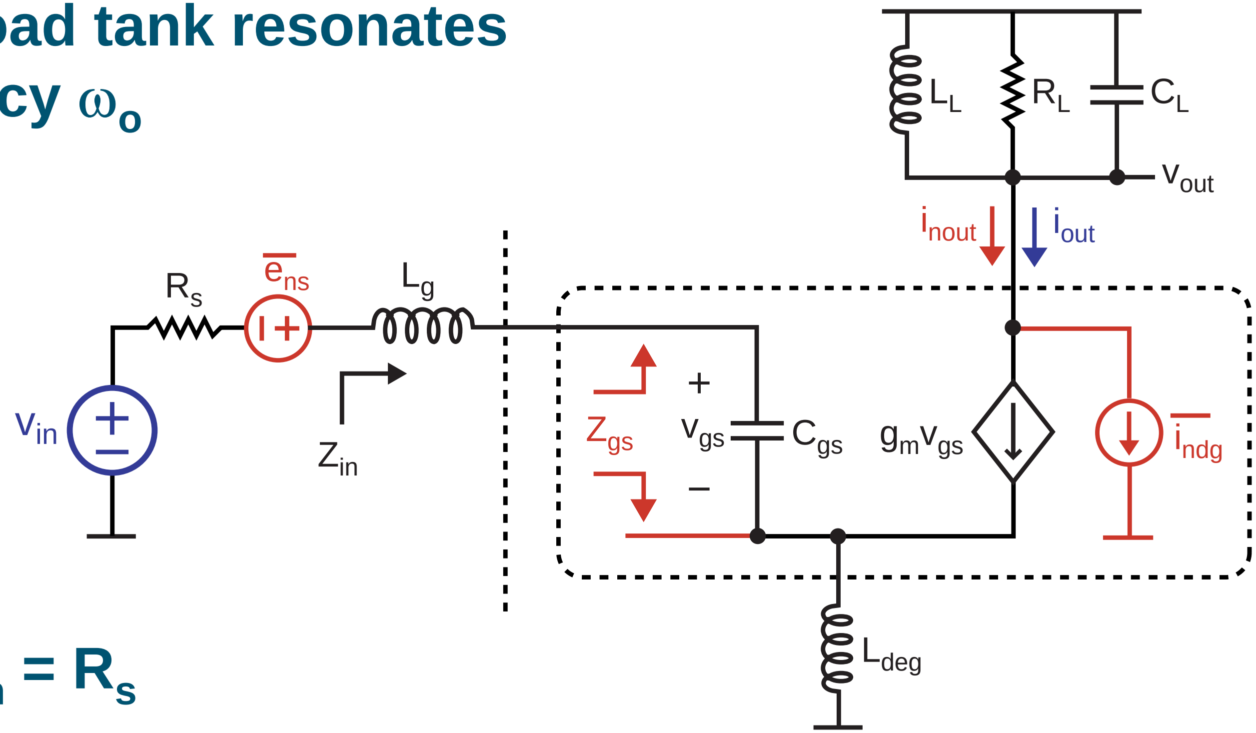
Inclusion of Load (Resonant Tank)

- **Add output load to achieve voltage gain**
  - **Note: in practice, use cascode device**
    - We're ignoring C_{gd} in this analysis



Calculation of Gain

- **Assume load tank resonates at frequency ω_o**



- **Assume $Z_{in} = R_s$**

$$\Rightarrow \quad v_{gs} = \frac{v_{in}}{2R_s}\left(\frac{1}{jw_oC_{gs}}\right) = \left(\frac{Q}{j}\right) v_{in}$$

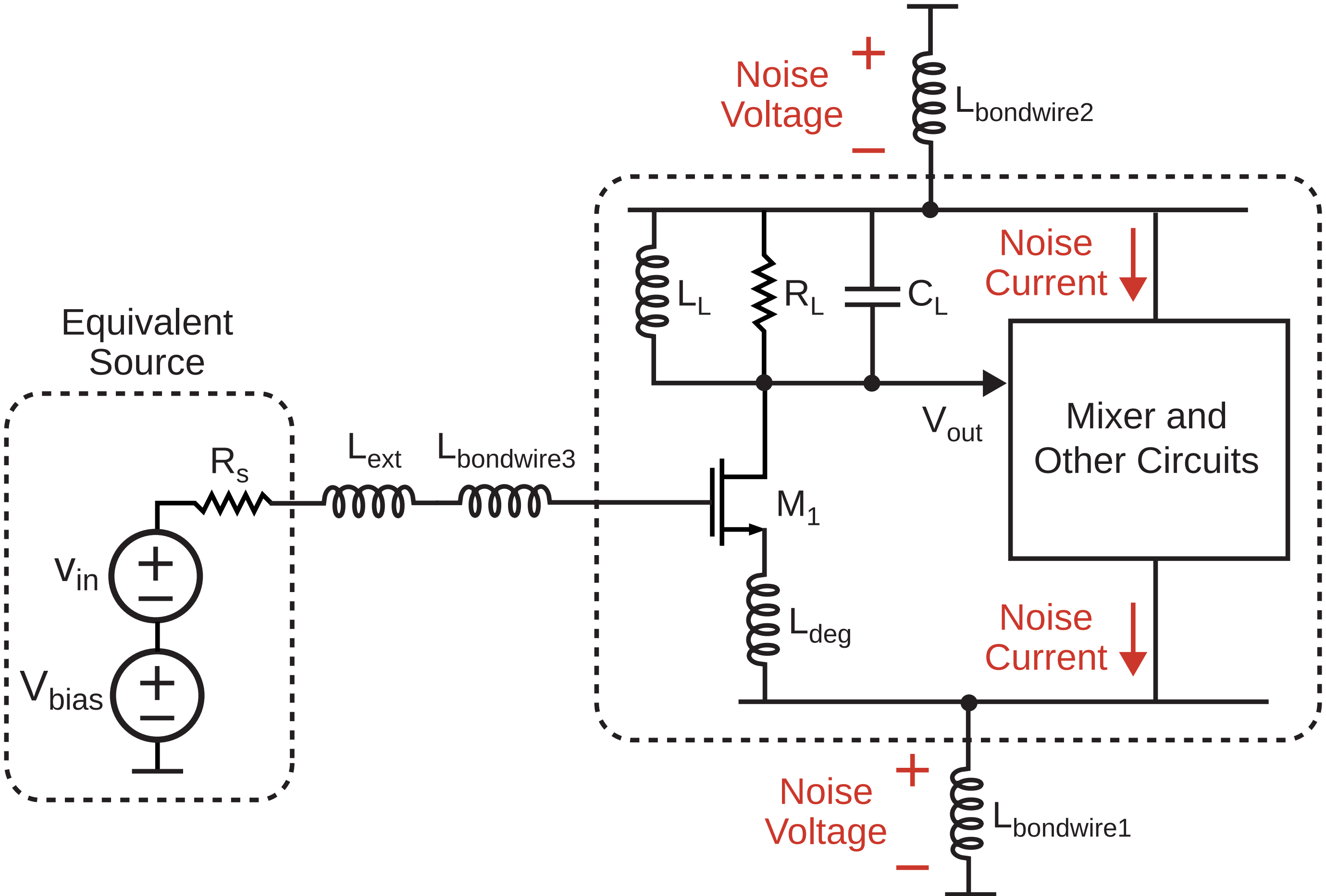
$$\Rightarrow \quad i_{out} = g_m \left(\frac{Q}{j}\right) v_{in} \qquad \Rightarrow \quad \boxed{v_{out} = -g_m R_L \left(\frac{Q}{j}\right) v_{in}}$$

Setting of Gain

$$|\text{Gain}| = g_m R_L Q$$

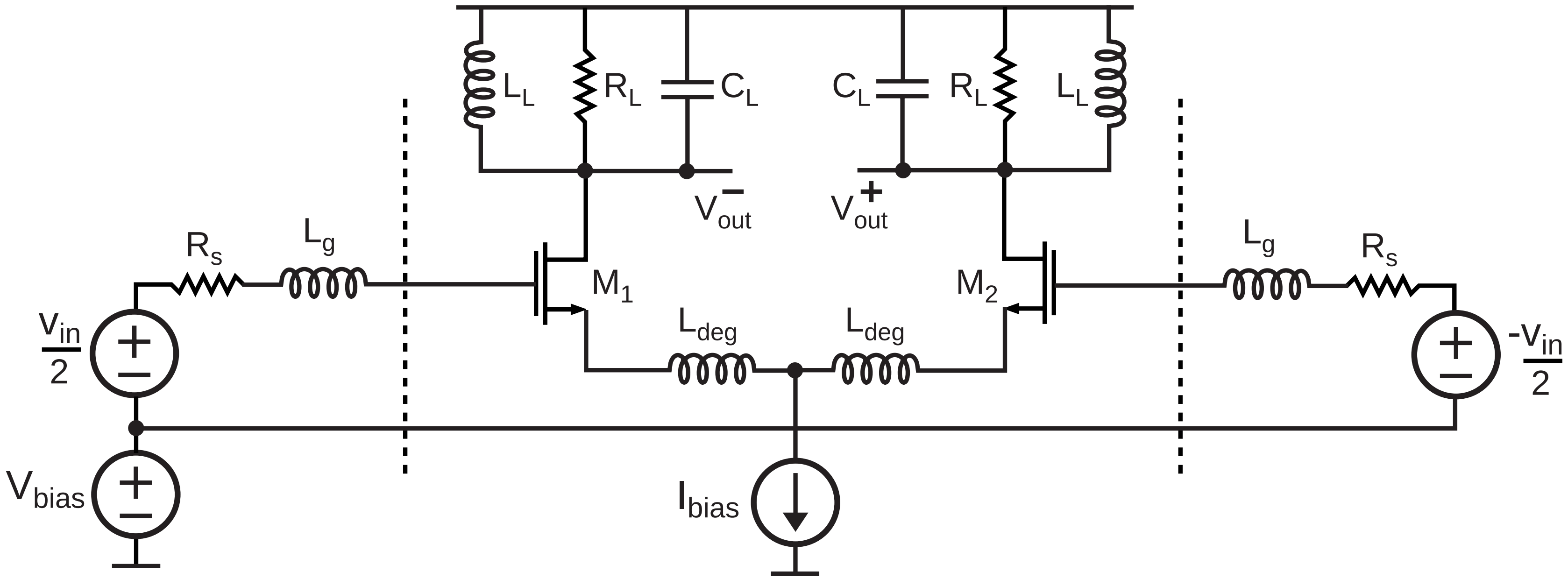
- **Parameters g_m and Q were set by Noise Figure and IIP3 considerations**
  - **Note that Q is of the input matching network, not the amplifier load**
- **R_L is the free parameter – use it to set the desired gain**
  - **Note that higher R_L for a given resonant frequency and capacitive load will increase Q_L (i.e., Q of the amplifier load)**
    - There is a tradeoff between amplifier bandwidth and gain
  - **Generally set R_L according to overall receiver noise and IIP3 requirements (higher gain is better for noise)**
    - Very large gain (i.e., high Q_L) is generally avoided to minimize sensitivity to process/temp variations that will shift the center frequency and to avoid parasitic oscillation

The Issue of Package Parasitics



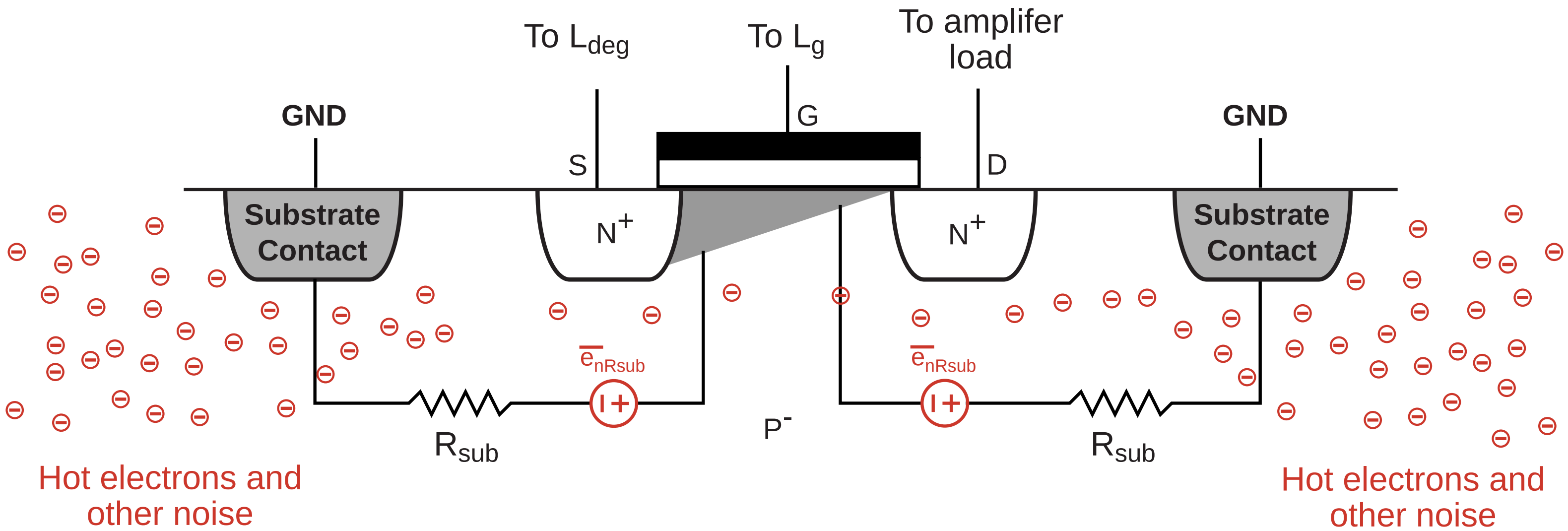
- Bondwire (and package) inductance causes two issues
  - Value of degeneration inductor is altered
  - Noise from other circuits couples into LNA

Differential LNA



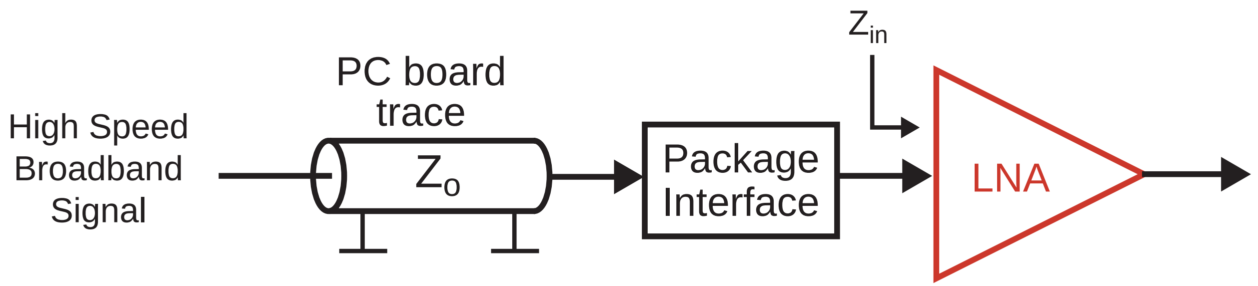
- **Advantages**
  - **Value of L_{deg} is now much better controlled**
  - **Much less sensitivity to noise from other circuits**
- **Disadvantages**
  - **Twice the power as the single-ended version**
  - **Requires differential input at the chip**

Note: Be Generous with Substrate Contact Placement



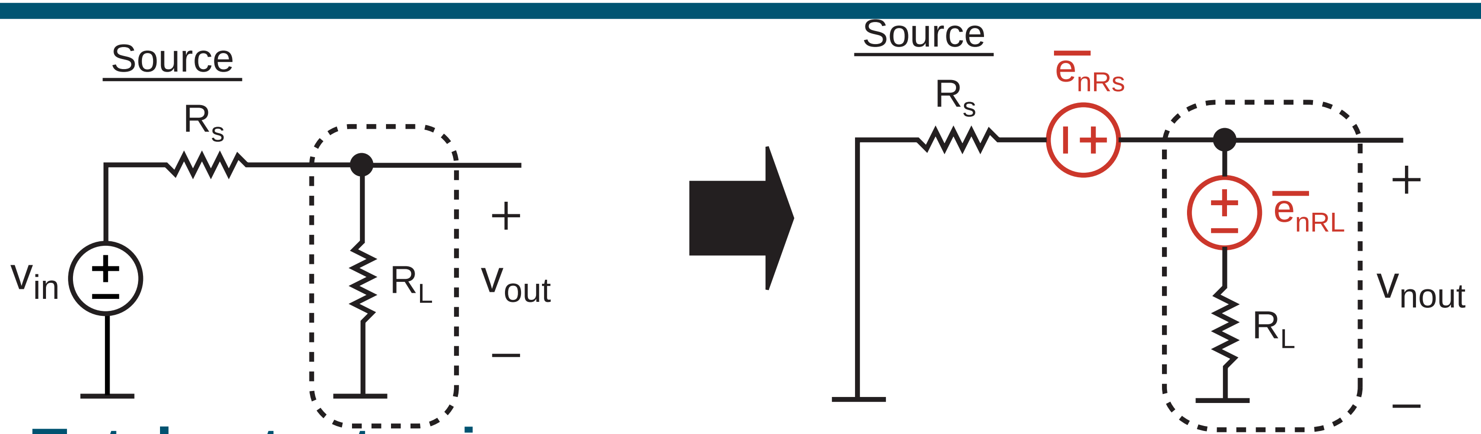
- **Having an abundance of nearby substrate contacts helps in three ways**
  - **Reduces possibility of latch up issues**
  - **Lowers R_{sub} and its associated noise**
    - Impacts LNA through backgate effect (g_{mb})
  - **Absorbs stray electrons from other circuits that will otherwise inject noise into the LNA**
- **Negative: takes up a bit extra area**

Broadband LNA Design



- Most broadband systems are not as stringent on their noise requirements as wireless counterparts
- Equivalent input voltage is often specified rather than a Noise Figure
- Typically use a resistor to achieve a broadband match to input source
  - We know from Lecture 12 that this will limit the noise figure to be higher than 3 dB
- For those cases where low Noise Figure is important, are there alternative ways to achieve a broadband match?

Recall Noise Factor Calculation for Resistor Load



- **Total output noise**

$$\overline{v^2_{nout(tot)}} = \left(\frac{R_L}{R_s+R_L}\right)^2 \overline{e^2_{nRs}} + \left(\frac{R_s}{R_s+R_L}\right)^2 \overline{e^2_{nRL}}$$

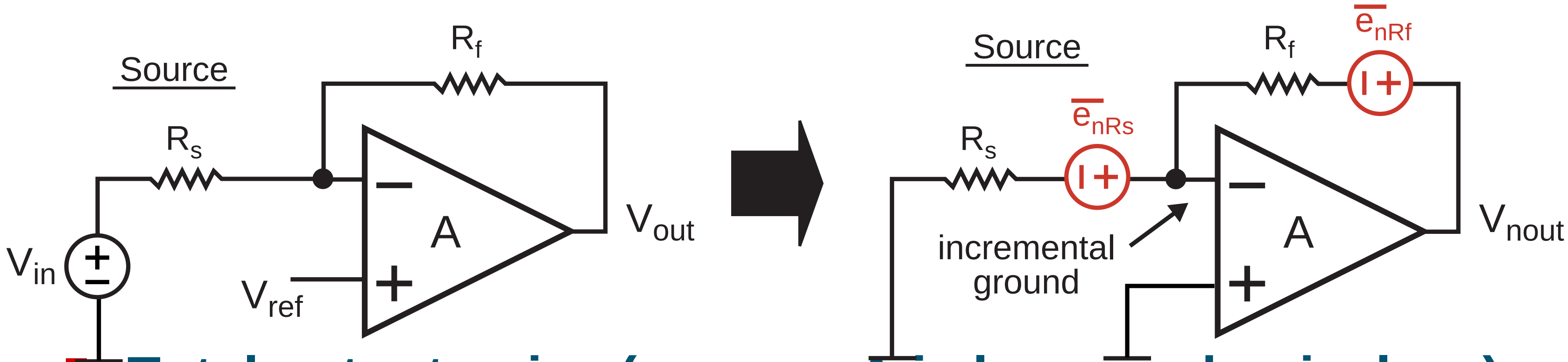
- **Total output noise due to source**

$$\overline{v^2_{nout(in)}} = \left(\frac{R_L}{R_s+R_L}\right)^2 \overline{e^2_{nRs}}$$

- **Noise Factor**

$$F = 1 + \left(\frac{R_s}{R_L}\right)^2 \frac{\overline{e^2_{nRL}}}{\overline{e^2_{nRs}}} = 1 + \left(\frac{R_s}{R_L}\right)^2 \frac{4kTR_L}{4kTR_s} = \boxed{1 + \frac{R_s}{R_L}}$$

Noise Figure For Amp with Resistor in Feedback



- **Total output noise (assume A is large and noiseless)**

$$\overline{v^2_{nout(tot)}} \approx \left(\frac{-R_f}{R_s}\right)^2 \overline{e^2_{nRs}} + \overline{e^2_{nRf}}$$

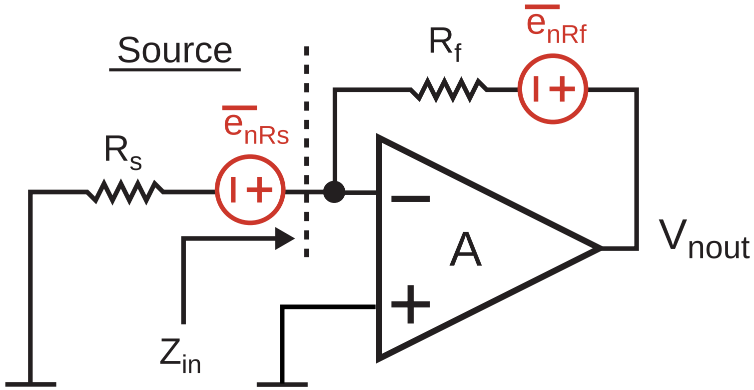
- **Total output noise due to source (assume A is large)**

$$\overline{v^2_{nout(in)}} \approx \left(\frac{-R_f}{R_s}\right)^2 \overline{e^2_{nRs}}$$

- **Noise Factor**

$$F \approx 1+\left(\frac{R_s}{R_f}\right)^2 \frac{\overline{e^2_{nRf}}}{\overline{e^2_{nRs}}} = 1+\left(\frac{R_s}{R_f}\right)^2 \frac{4kTR_f}{4kTR_s} = \boxed{1+\frac{R_s}{R_f}}$$

Input Impedance For Amp with Resistor in Feedback



- **Recall from Miller effect discussion that**

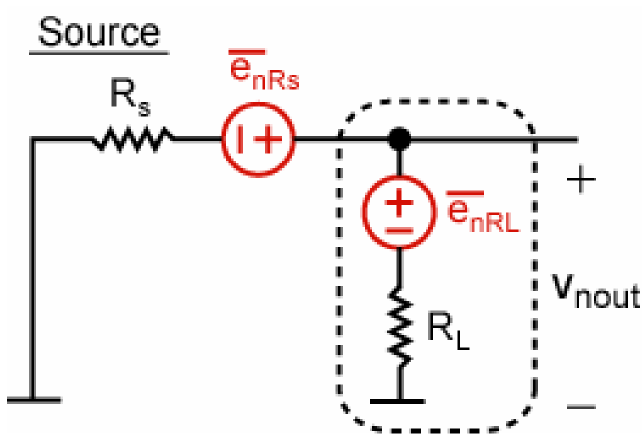
$$Z_{in} = \frac{Z_f}{1 - gain} = \frac{R_f}{1 + A}$$

- **If we choose Z_{in} to match R_s, then**

$$R_f = (1 + A)Z_{in} = (1 + A)R_s$$

- **Therefore, Noise Figure lowered by being able to choose a large value for R_f since** $F \approx 1 + \frac{R_s}{R_f}$

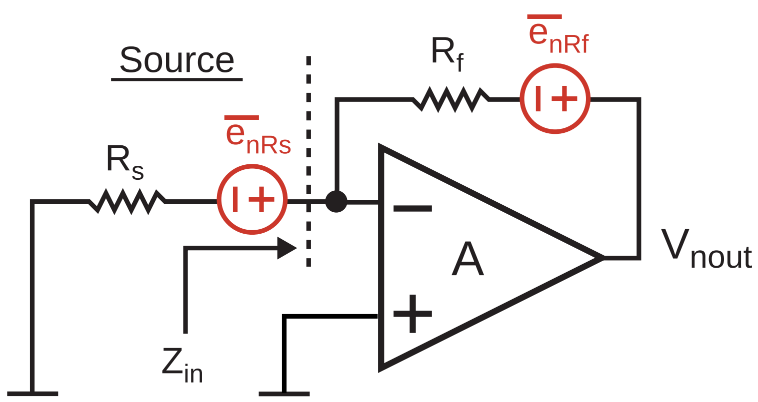
Resistor Termination vs. Resistor in Feedback



For Termination

$$R_s = R_L$$

$$F \approx 1 + \frac{R_s}{R_L} = 2$$

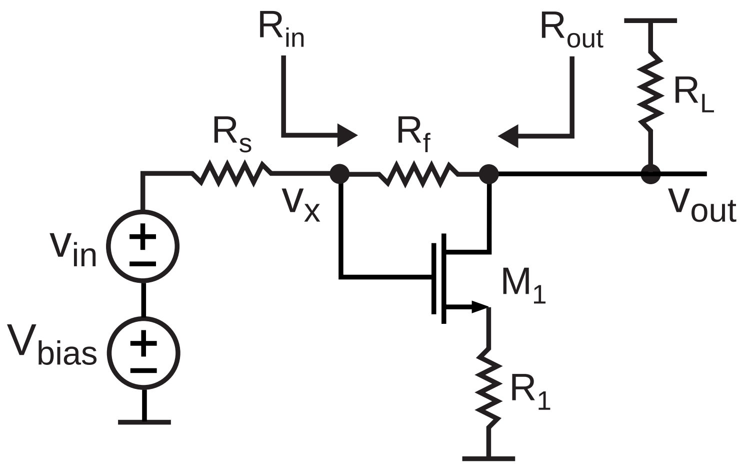


For Termination

$$R_f = (1 + A)Z_{in} = (1 + A)R_s$$

$$F \approx 1 + \frac{R_s}{R_f} = 1 + \frac{1}{1 + A}$$

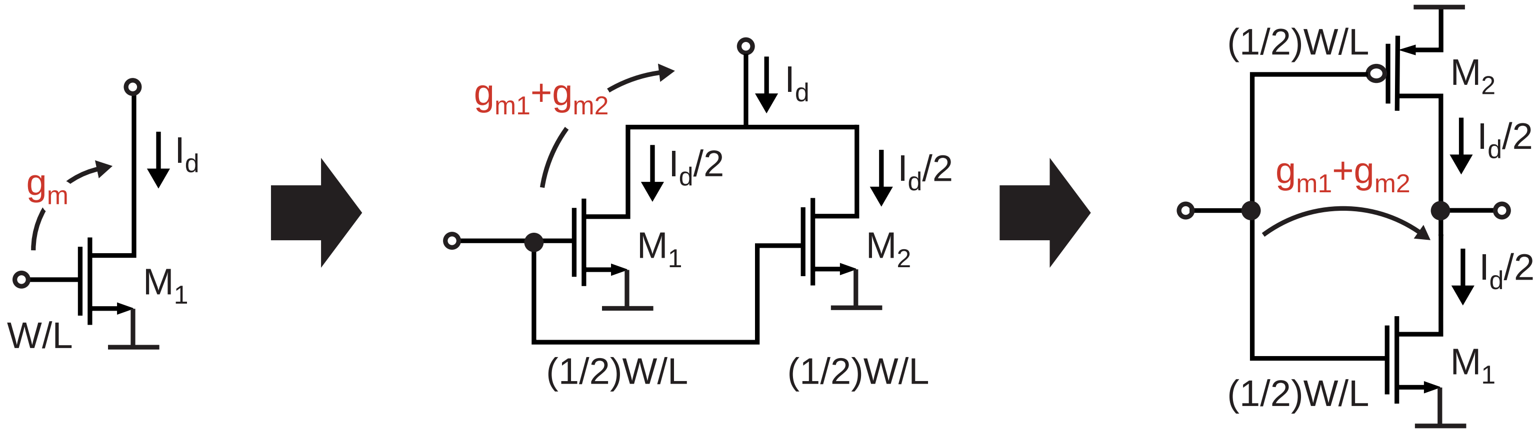
Example – Series-Shunt Amplifier



- **Recall that the above amplifier was analyzed in Lecture 7**
- **Tom Lee's book points out that this amplifier topology is actually used in noise figure measurement systems such as the Hewlett-Packard 8970A**
  - **It is likely to be a much higher performance transistor than a CMOS device, though**

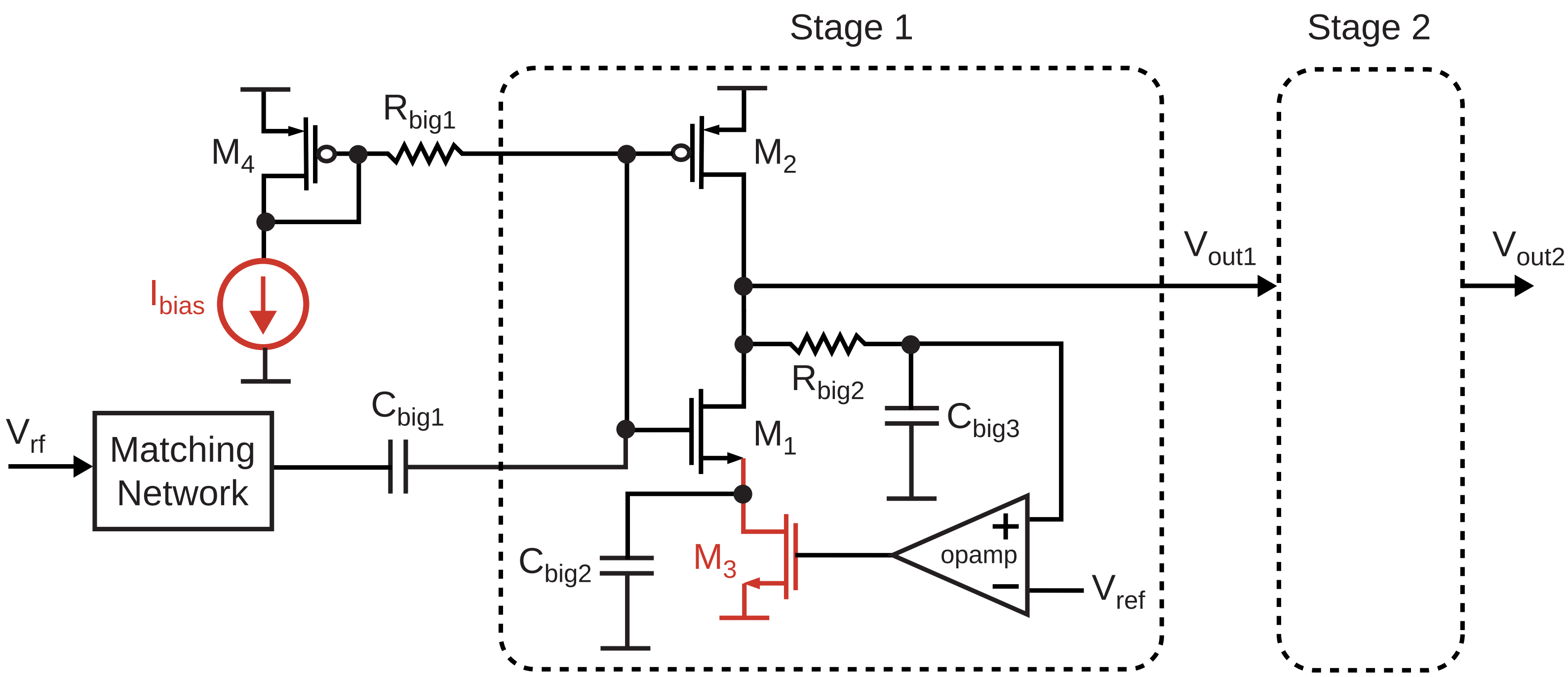
Recent CMOS LNA Techniques

- **Consider increasing g_m for a given current by using both PMOS and NMOS devices**
  - **Key idea: re-use of current**



See A. Karanicolas, "A 2.7 V 900-MHz CMOS LNA and Mixer", JSSC, Dec 1996

Biasing for LNA Employing Current Re-Use



- **PMOS is biased using a current mirror**
- **NMOS current adjusted to match the PMOS current**

Another Recent Approach

- **Feedback from output to base of transistor provides another degree of freedom. Negative feedback improves IIP3**

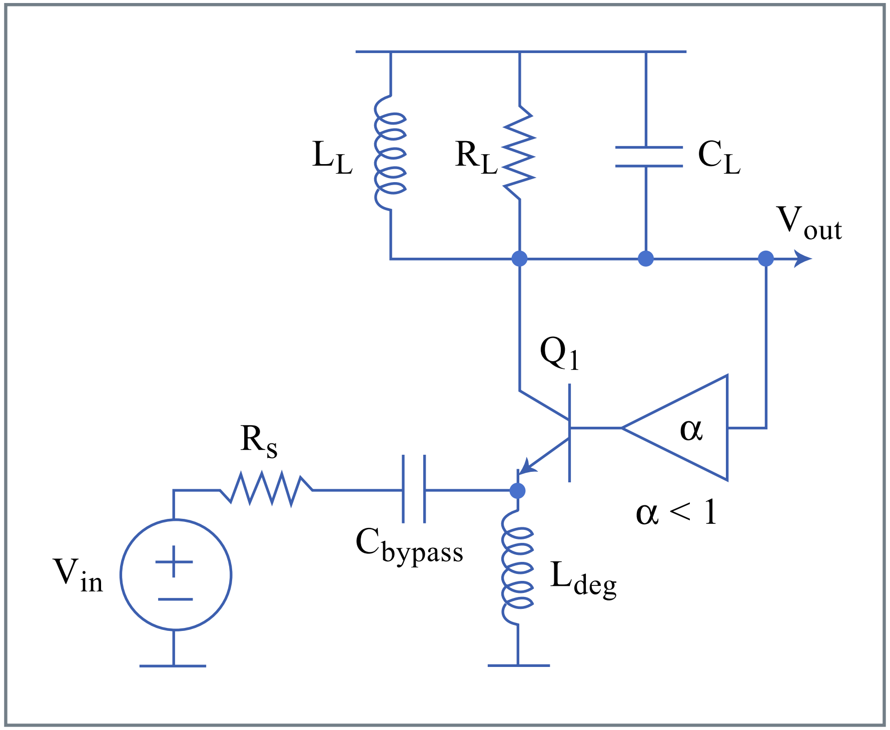
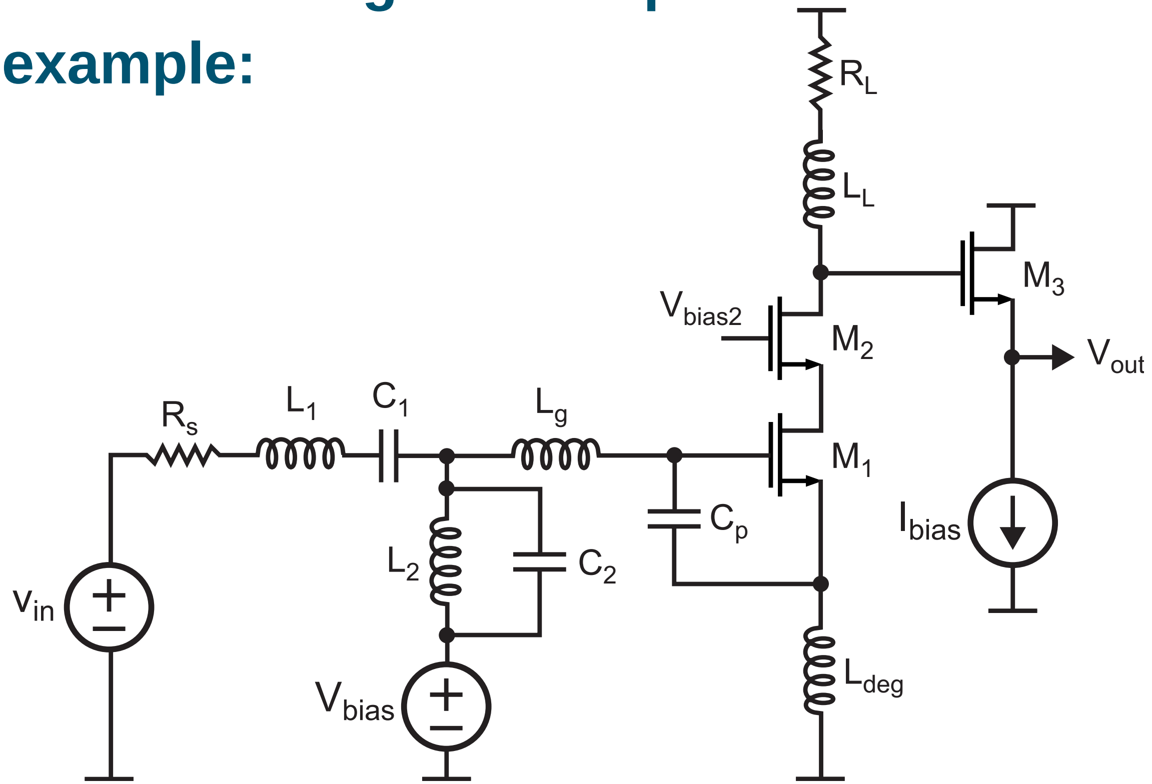


Figure by MIT OCW.

- **For details, check out:**
  - **Rossi, P. et. Al., “A 2.5 dB NF Direct-Conversion Receiver Front-End for HiperLan2/IEEE802.11a”, ISSCC 2004, pp. 102-103**

Recent Broadband LNA Approaches

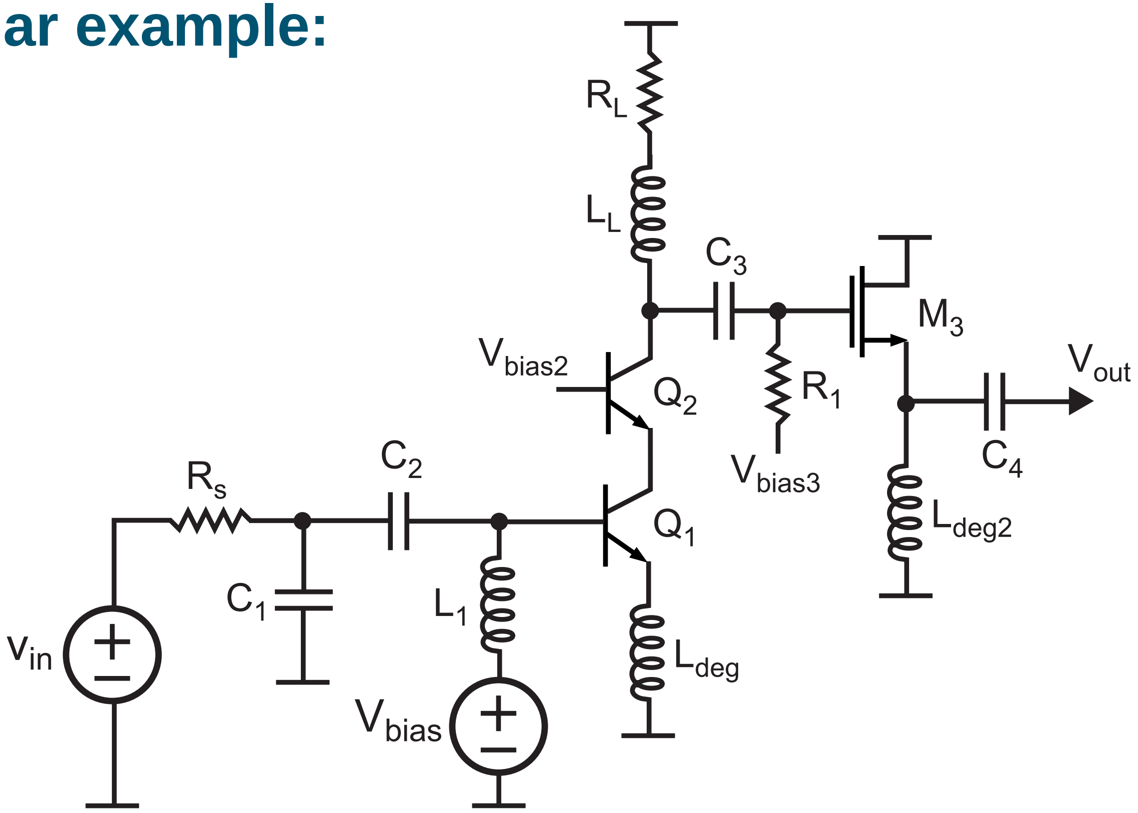
- **Can create broadband matching networks using LC-ladder filter design techniques**
- **CMOS example:**



- **See Bevilacqua et. al, "An Ultra-Wideband CMOS LNA for 3.1 to 10.6 GHz Wireless Receivers", ISSC 2004, pp. 382-383**

Recent Broadband LNA Approaches (Continued)

- **Bipolar example:**



- **See Ismail et. al., "A 3 to 10 GHz LNA Using a Wideband LC-ladder Matching Network", ISSCC 2004, pp. 384-385**

Gm Boosting for Noise Figure Improvement

- **Gm Boosted CG Amp**

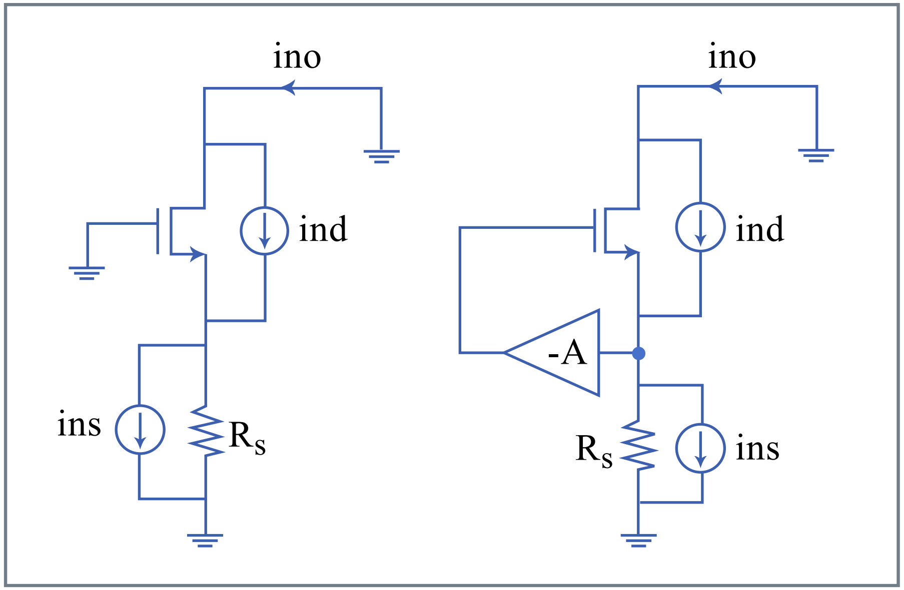


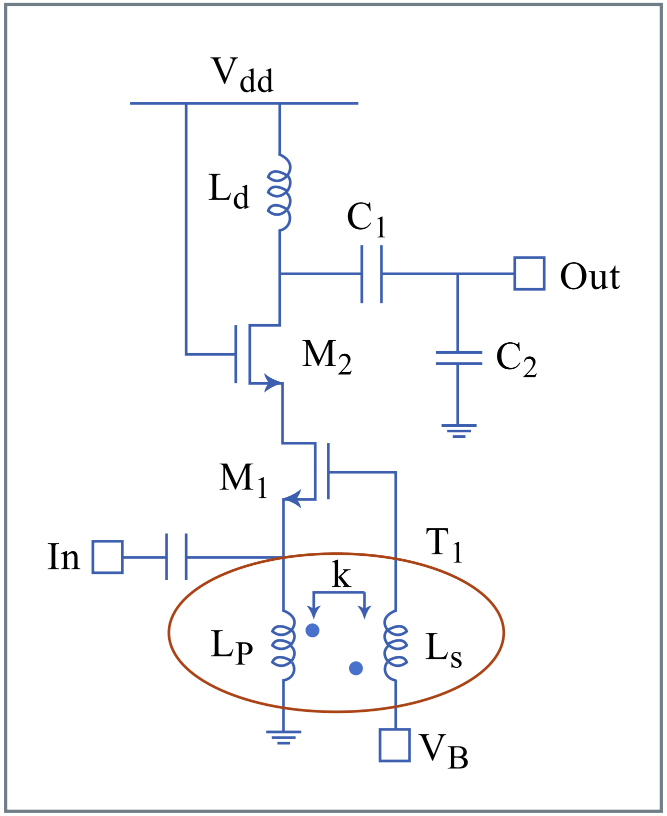
Figure by MIT OCW.

$$F = 1 + \frac{\gamma}{\alpha} \qquad F = 1 + \frac{\gamma}{\alpha} \cdot \frac{1}{1 + A}$$

But, the amplifier adds noise and power. How do we boost the Gm without an amplifier?

- **See Xiaoyong Li et. al., "Low-Power gm-boosted LNA and VCO Circuits in 0.18μm CMOS" 2005 ISSCC Digest of Technical Papers pp. 534-353**

Gm Boosting by a Transformer

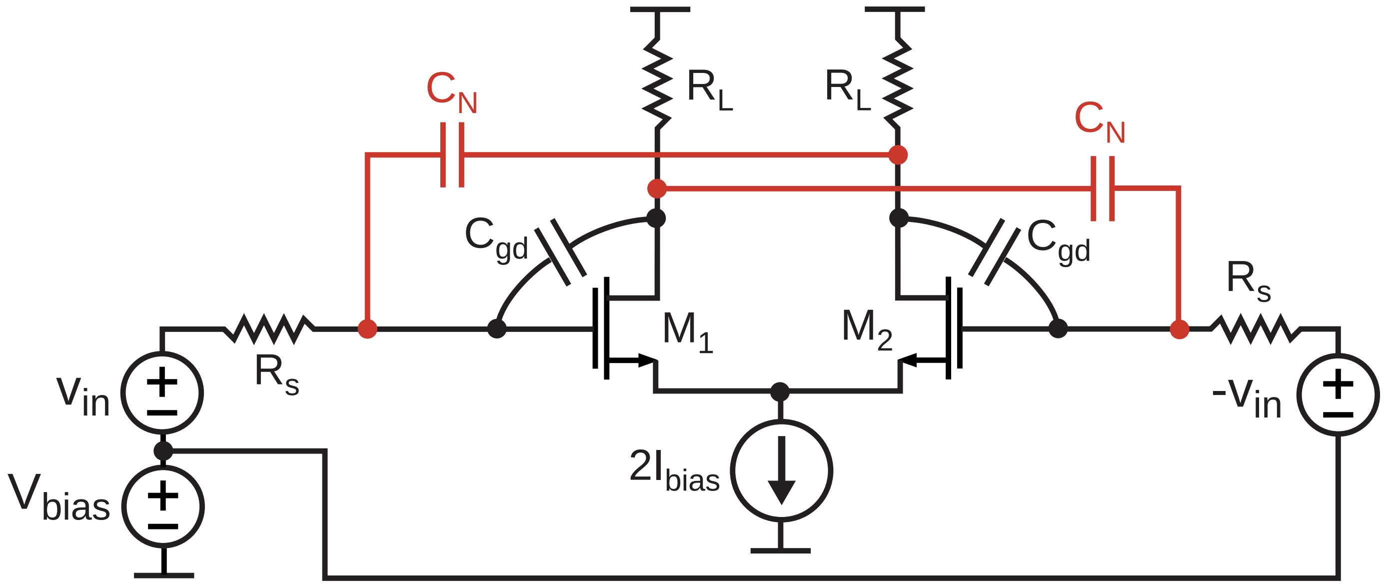


$$F = 1 + \frac{\gamma}{\alpha} \cdot \frac{1}{1+nk}$$

Figure by MIT OCW.

- **Gm is boosted without adding noise by the step-up transformer**
- **Transformer provides gate and source with voltages 180º out of phase: effective increase in V_{gs}**

Revisit Neutralizaton



- Issues:
  - Power Consumption
  - Output swing (additional drop for the tail current)
  - Differential output
  - Matching between C_{gd} and C_N

Can We Tune Out C_{gd} Instead?

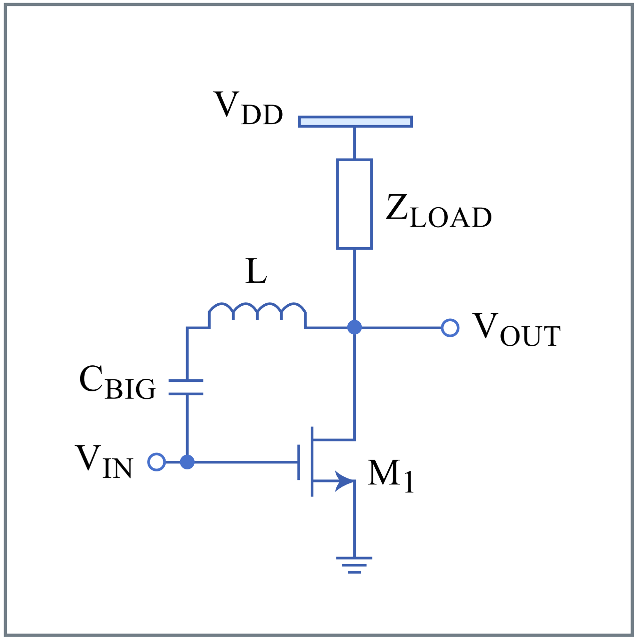


Figure by MIT OCW.

- **Conceptually, one can tune out C_{gd} by a series inductor L. C_{BIG} is necessary to block DC between input and output.**
  - **Inductor value too large**
  - **Bottom plate parasitic capacitance of C_{BIG}**

Source: David J. Cassan , et. al., “A 1-V Transformer-Feedback Low-Noise Amplifier for 5-GHz Wireless LAN in 0.18 m CMOS” IEEE J. Solid-State Circuits, vol. SC-23 pp 427-435, Mar. 2003

Neutralization by Transformer Feedback

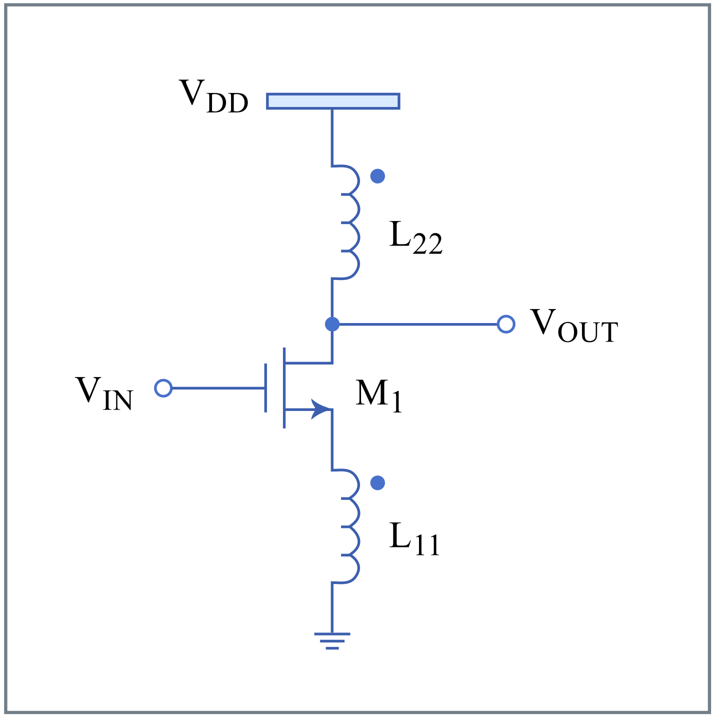


Figure by MIT OCW.

Neutraliztion of C_{gd} by C_{gs} if

$$\frac{n}{k} = \frac{C_{gs}}{C_{gd}}$$

- Advantages
  - No DC drop: can operate at low supply voltages
  - Power match by inductor degeneration
  - No additional power consumption
  - C_{gd} to C_{gs} matching is better than C_{gd} to C_N

Differential Implementation

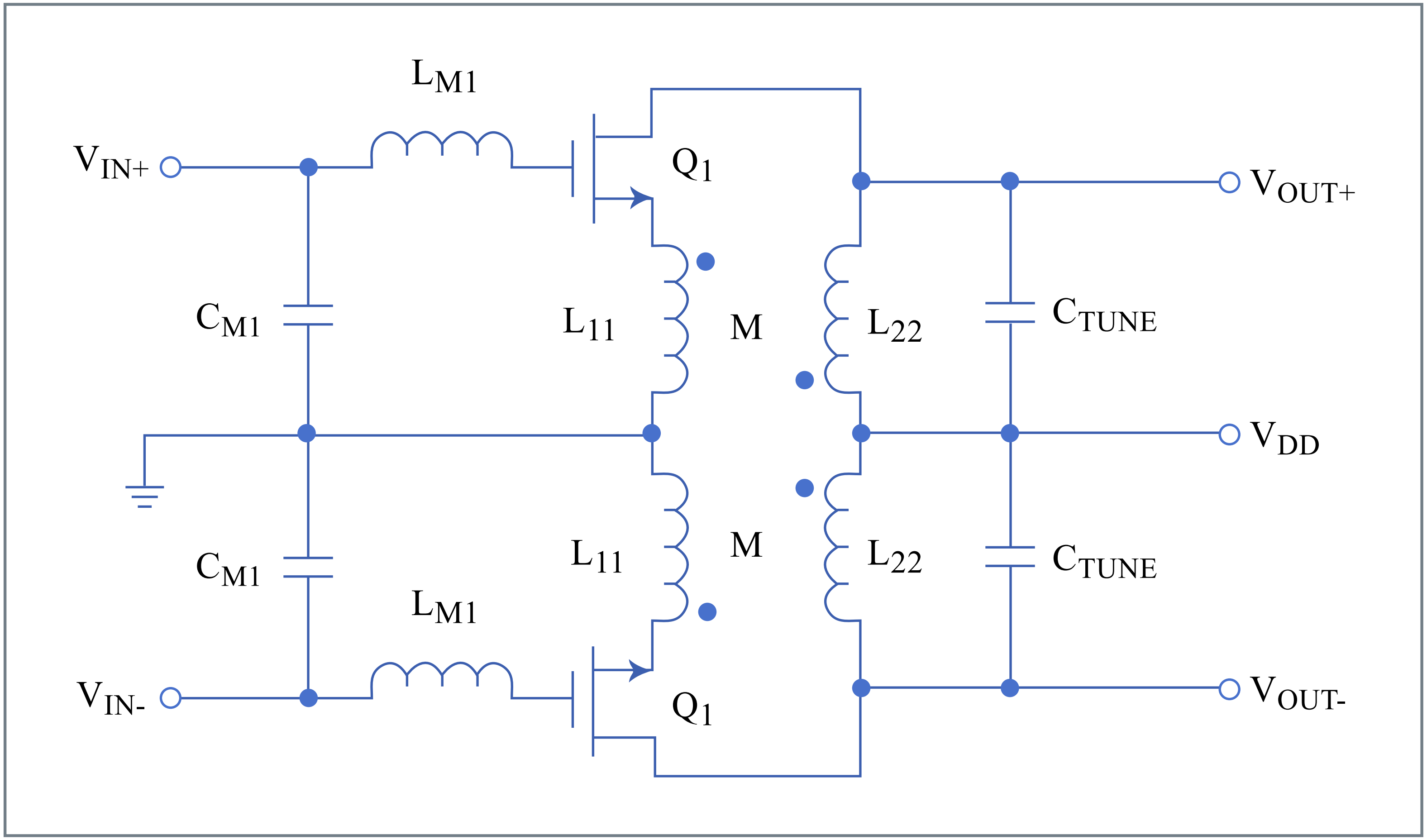


Figure by MIT OCW.

See David J. Cassan , et. al., "A 1-V Transformer-Feedback Low-Noise Amplifier for 5-GHz Wireless LAN in 0.18 m CMOS" IEEE J. Solid-State Circuits, vol. SC-23 pp 427-435, Mar. 2003

Differential Output LNA

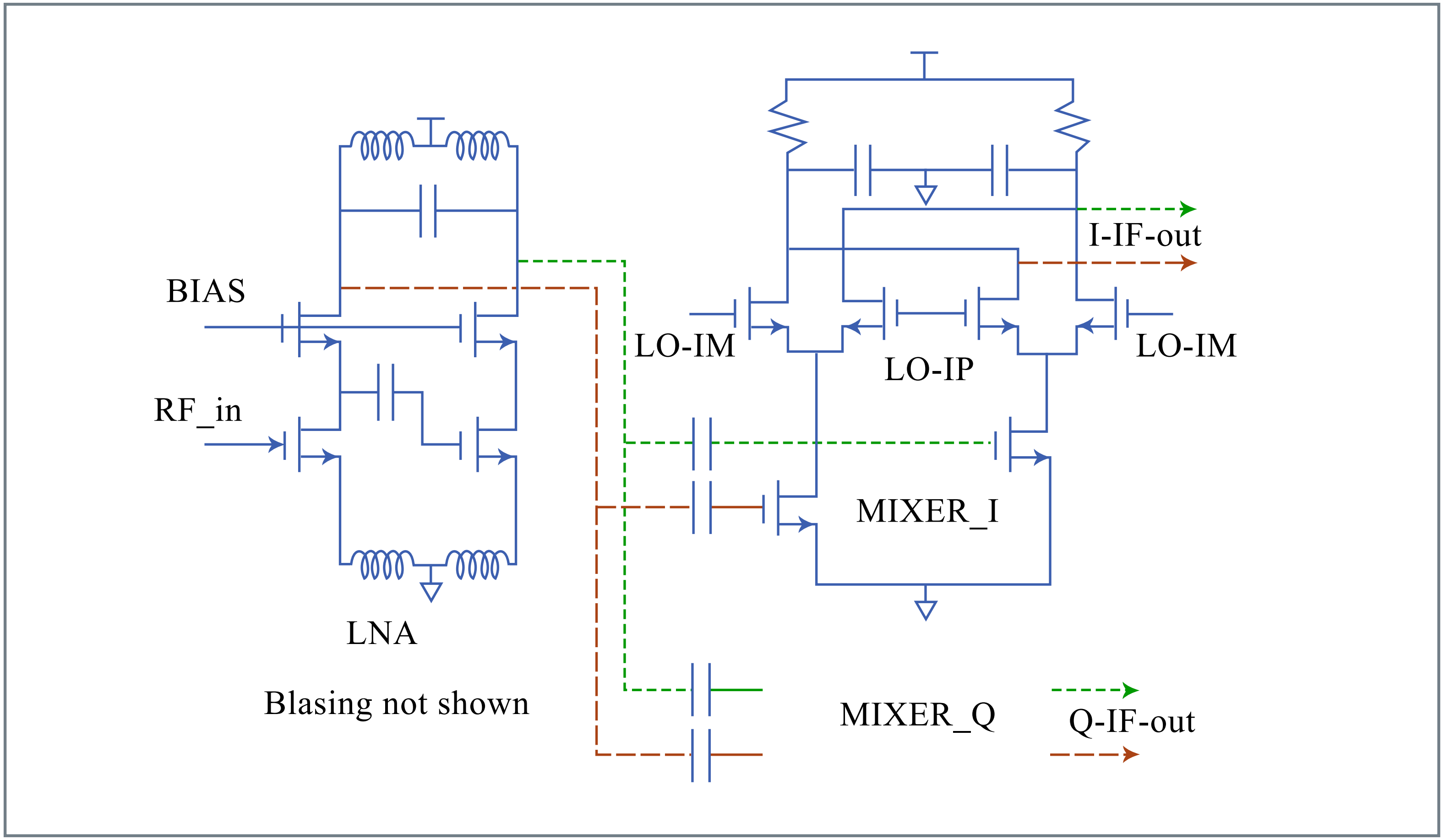


Figure by MIT OCW.

Provides differential output to drive balanced mixers

See D. Sahu et. al. "A 90nm CMOS Single-Chip GPS Receiver with 5dBm Out-of-Band IIP3 2.0dB NF", 2005 ISSCC Digest of Technical Papers, pp308-309

Adjustable Gain LNA

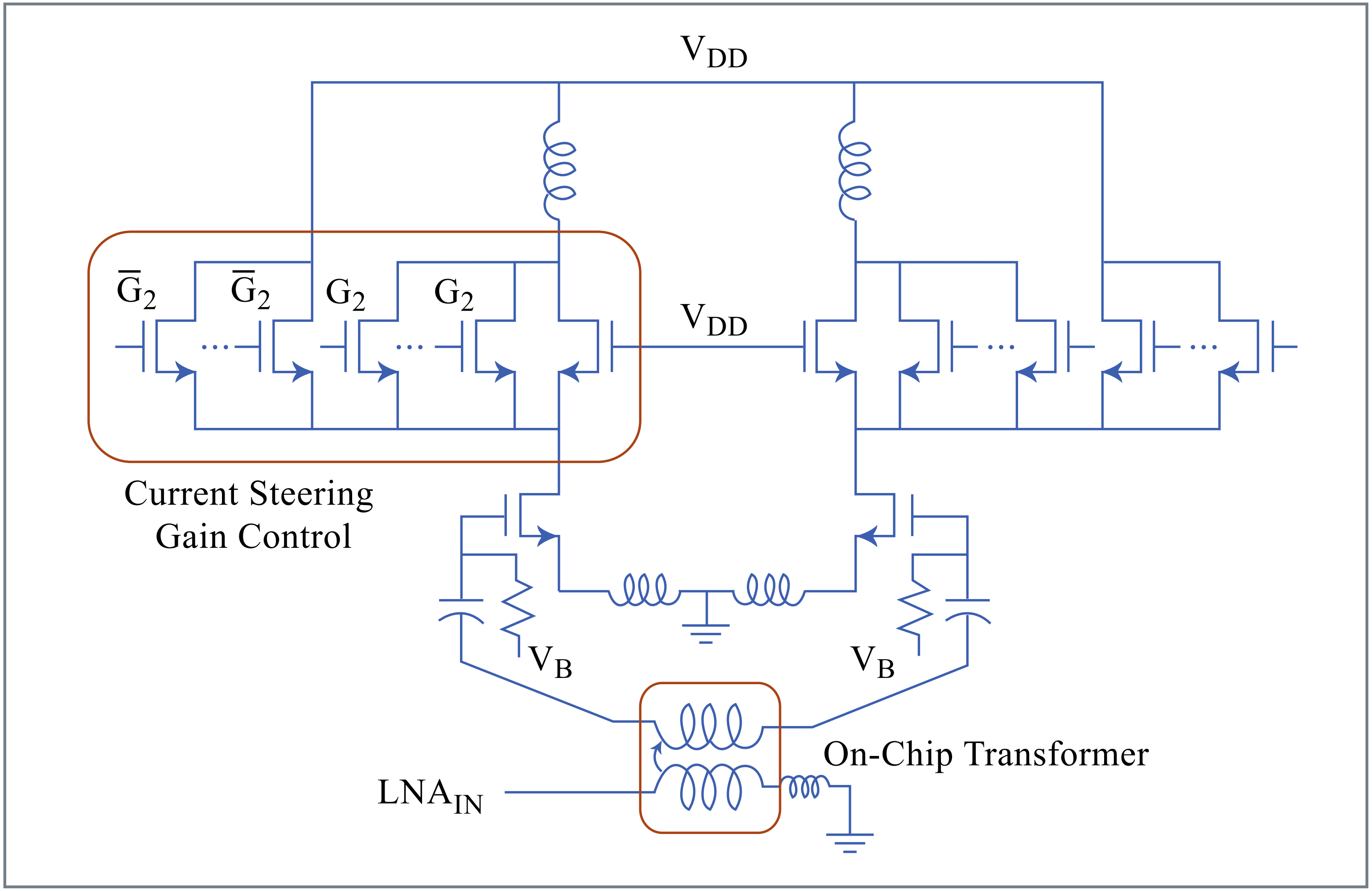


Figure by MIT OCW.

Gain is adjusted by diverting output current in the cascode stage

See H. Darabi, et. al, "A Fully Integrated SoC for 802.11b in 0.18µm CMOS", 2005 ISSCC Digest of Technical Papers, pp 96-97.