

6.776
High Speed Communication Circuits
Spring 2005

Homework #2: S -parameters, Impedance Transformers, and Smith Charts
Passed Out: February 15, 2005 Due: February 24, 2005

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Reading: Chapters 4-6 of Thomas H. Lee's book (First Edition) **OR**
Chapters 3,6,7 of Thomas H. Lee's book (Second Edition)

1. Consider the high speed trace and its associated two-port model shown in Figure 1. In the model, the transmission line corresponds to an RF connector and PCB trace (both assumed to be ideal), C_1 is the capacitance of the package pin to the package substrate and adjoining pins, L_1 is the bondwire inductance, C_2 is the on-chip pad capacitance, and R_L is the on-chip termination resistor. For all calculations to follow, it assumed that the source driving impedance is precisely matched to the transmission line characteristic impedance, R_o .

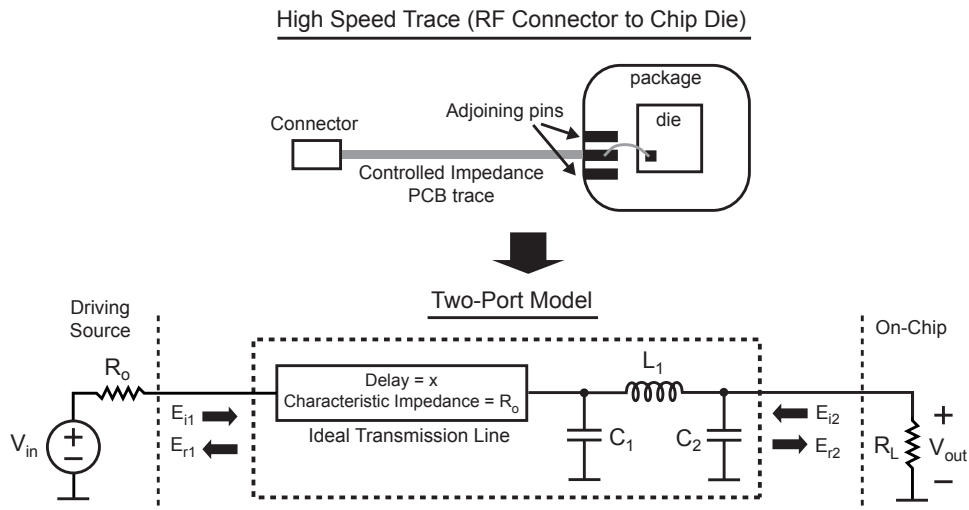


Figure 1: Example high speed trace and associated 2-port model.

Calculate S_{11} and S_{21} for each of the following cases:

- (a) $R_o = 50$ Ohms, $x = 0$ ps, $C_1 = 0.0$ pF, $L_1 = 0$ nH, $C_2 = 0$ pF, $R_L = 65$ Ohms
- (b) $R_o = 50$ Ohms, $x = 0$ ps, $C_1 = 0.0$ pF, $L_1 = 0$ nH, $C_2 = 5$ pF, $R_L = 65$ Ohms
- (c) $R_o = 50$ Ohms, $x = 200$ ps, $C_1 = 0.0$ pF, $L_1 = 0$ nH, $C_2 = 5$ pF, $R_L = 65$ Ohms

- (d) $R_o = Z_o$, $x = \text{delay}$, $C_1 = C_1$, $L_1 = L_1$, $C_2 = C_2$, $R_L = Z_L$
2. The following problem is taken from problem 2 of Chapter 4 from Thomas Lee's book (First Edition). Suppose we wish to deliver 1 Watt of power into a 50 Ohm load at 1.8 GHz, but are constrained to using a power amplifier that has a peak-to-peak sinusoidal voltage of only 2.5 V due to transistor breakdown issues. Design the following matching networks to allow 1 W to be delivered in two ways: 1) using the equations derived in the course notes and 2) using a Smith Chart. Use lowpass versions in all cases, and assume that all reactive elements are ideal. You can download blank Smith Charts from the **Study materials** section.
 - (a) L-match
 - (b) π -match ($Q = 12$)
 - (c) T-match ($Q = 12$)
 - (d) Tapped capacitor ($Q = 12$)
 - (e) If the maximum allowable on-chip capacitance is 200 pF and the maximum allowable on-chip inductance is 20 nH, are any of your designs amenable to a fully integrated implementation? If so, which one(s)?
 3. Simulate the transformer networks computed in Problem 2 using Spectre on MIT server. Be sure to use Cadence for design entry as specified in the documents handed out in class. Assume that the source driving impedance is a resistor that matches the nominal input impedance of the transformer at 1.8 GHz. Adjust the input source voltage such that 2.5 V peak-to-peak occurs at the inputs of the transformer networks.

Based on the Spectre results, compute and plot S_{11} and S_{21} of each transformer network (from transformer input to output) across the frequency range of 1.5 GHz to 2.1 GHz. Comment on the differences between the performance of each transformer. (Note: you should reference the input as the signal source rather than the input to the transformer - why?)
 4. Now consider the high speed trace and it's associated two-port model shown in Figure 2, which is similar to that examined in Problem 1. In this case, we will focus only on the relationship between the transmission line parameters and the physical PCB characteristics.
 - (a) Assuming that the PCB trace is a 0.5 ounce Microstrip Trace whose dielectric has $\epsilon_r = 4.3$ and a height of 12 mils, use the web-based tool at <http://www.emclab.umr.edu/pcbtlc> to perform the following calculations.
 - i. Determine the required width of the PCB trace to achieve 50 Ohms characteristic impedance.
 - ii. Calculate how long the trace must be to match the assumed propagation delay of 150 ps.

High Speed Trace (RF Connector to Chip Die)

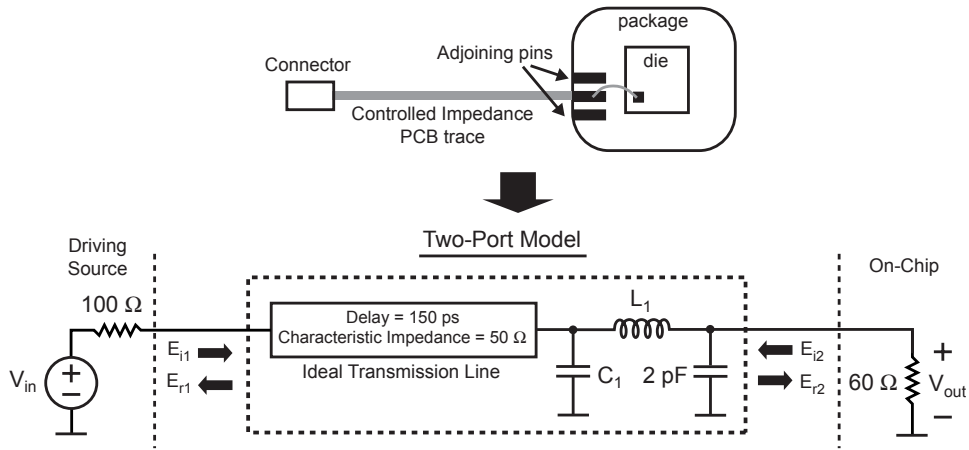


Figure 2: Example high speed trace and associated 2-port model.

- (b) Repeat (a) for a Stripline Trace under the assumption that each dielectric thickness has the same ϵ_r and height of 12 mils.
- (c) What would be the advantages and disadvantages of using a Microstrip Trace versus a Stripline Trace for high speed signaling applications?