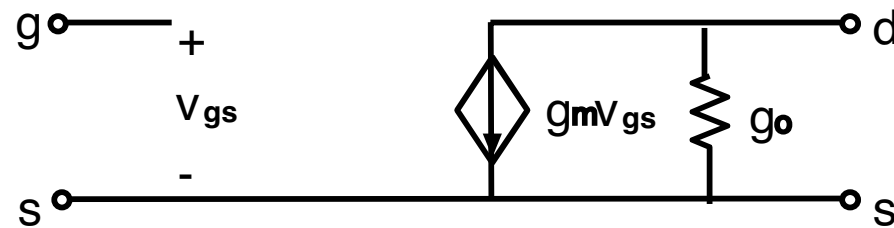


Lecture 10 - MESFET IC Applications - Outline

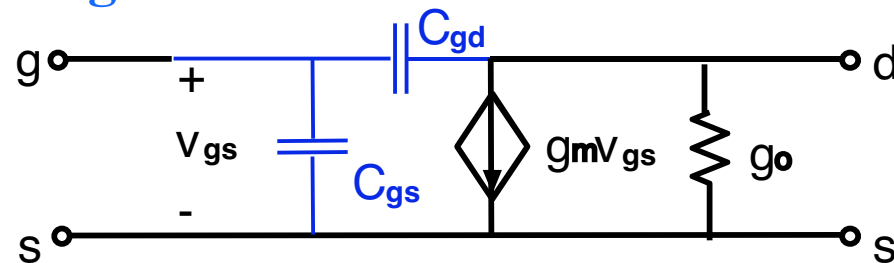
- **Left over items from Lect. 9**
 - High frequency model and performance
 - Processing technology
- **Monolithic Microwave Integrated Circuits**
 - General concept
 - Microstrip layout; Discrete components
 - Specific examples
 - Mesa etched; Ion implanted
- **Digital Logic**
 - The difficulty of using depletion-mode transistors
 - General comments
 - Logic families
 - FET logic; Buffered FET logic (BFL); Schottky diode FET logic (SDFL)
 - Direct-coupled FET logic (DCFL)
 - Complementary FET logic (none exists, or is likely to anytime soon)
 - Other building blocks
 - Transfer gates
 - Memory cells

Linear equivalent circuit models - schematics

In Lecture 9 we developed a small signal linear equivalent circuit for the MESFET; it can be drawn as:



To extend this model to high frequencies we introduce small signal linear capacitors representing the charge stored on the gate:



$$C_{gs} \equiv \left. \frac{\partial q_G}{\partial v_{GS}} \right|_Q$$

$$C_{gd} \equiv \left. \frac{\partial q_G}{\partial v_{DS}} \right|_Q$$

MESFET - linear equivalent circuit, cont

For a MESFET biased in saturation, we find the following expressions for the conductances in the small signal equivalent circuit model:

$$g_i \equiv \left. \frac{\partial i_G}{\partial v_{GS}} \right|_Q = 0 \quad g_r \equiv \left. \frac{\partial i_G}{\partial v_{DS}} \right|_Q = 0$$

$$g_m \equiv \left. \frac{\partial i_D}{\partial v_{GS}} \right|_Q = G_o \left[1 - \sqrt{\frac{(\phi_b - V_{GS})}{(\phi_b - V_P)}} \right]$$

$$g_o \equiv \left. \frac{\partial i_D}{\partial v_{DS}} \right|_Q \approx \lambda I_D = I_D / V_A$$

The intrinsic gate-to-drain capacitance, C_{gd} , is 0 in saturation, but in a real device there is a small, parasitic (extrinsic) C_{gd} ; the value is determined empirically.

The intrinsic gate-to-source capacitance, C_{gs} , is dq_G/dv_{GS} , where the gate charge, q_G , is:

$$q_G = W q N_{Dn} \int_0^L x_d(y) dy$$

Not easy to evaluate!

Impact of velocity saturation - Model A'

Consider a MESFET with such a short channel that the carriers reach their saturation velocity at very small v_{DS} . The voltage drop along the channel will be small and the depletion region width under the gate will be uniform:

$$x_d(y) \approx x_d(0) = \sqrt{2\varepsilon_s(\phi_b - v_{GS})/qN_{Dn}}$$

In such a device, the current will be that in a uniform resistor when v_{DS} is small:

$$i_D \approx W q N_{Dn} [a - x_d(0)] \mu_e v_{DS} / L = W q N_{Dn} \left[a - \sqrt{2\varepsilon_s(\phi_b - v_{GS})/qN_{Dn}} \right] \mu_e v_{DS} / L$$

$$\text{for } v_{DS} \leq L s_{sat} / \mu_e$$

In saturation the electrons in the channel will be moving at their saturation velocity, s_{sat} , and the current will be:

$$i_D \approx W q N_{Dn} [a - x_d(0)] s_{sat} = W q N_{Dn} \left[a - \sqrt{2\varepsilon_s(\phi_b - v_{GS})/qN_{Dn}} \right] s_{sat}$$

$$\text{for } v_{DS} \geq L s_{sat} / \mu_e$$

Cont. on next slide...

Impact of velocity saturation - Model A', cont.

Continuing with the short, velocity saturated MESFET, we can use our earlier definitions of G_o and V_P to write the drain current at low v_{DS} as:

$$i_D = G_o \left[1 - \sqrt{\frac{(\phi_b - v_{GS})}{(\phi_b - V_P)}} \right] v_{DS} \quad \text{for } v_{DS} \leq Ls_{sat} / \mu_e$$

And, in saturation the current is:

$$i_D = G_o \left[1 - \sqrt{\frac{(\phi_b - v_{GS})}{(\phi_b - V_P)}} \right] \frac{Ls_{sat}}{\mu_e} \quad \text{for } v_{DS} \geq Ls_{sat} / \mu_e$$

The linear equivalent circuit transconductance in this device when it is biased in saturation is:

$$\begin{aligned} g_m &\equiv \partial i_D / \partial v_{GS} \Big|_Q = W s_{sat} \sqrt{\epsilon_s q N_{Dn} / 2(\phi_b - V_{GS})} \\ &= G_o Ls_{sat} / \mu_e \sqrt{2(\phi_b - V_{GS})(\phi_b - V_P)} \end{aligned}$$

Impact of velocity saturation - Model A', cont.

Before continuing we can first compare this result with the earlier result for a MESFET with no velocity saturation:

$$\text{With no velocity saturation : } g_m = G_o \left[\frac{\sqrt{(\phi_b - V_P)} - \sqrt{(\phi_b - V_{GS})}}{\sqrt{(\phi_b - V_P)}} \right]$$

$$\text{With strong velocity saturation : } g_m = \frac{G_o L s_{sat}}{\mu_e \sqrt{2(\phi_b - V_{GS})(\phi_b - V_P)}}$$

Finally, turn to the incremental gate-to-source capacitance. It is easy to calculate in this model. We begin by finding the charge on the gate, and then differentiate it:

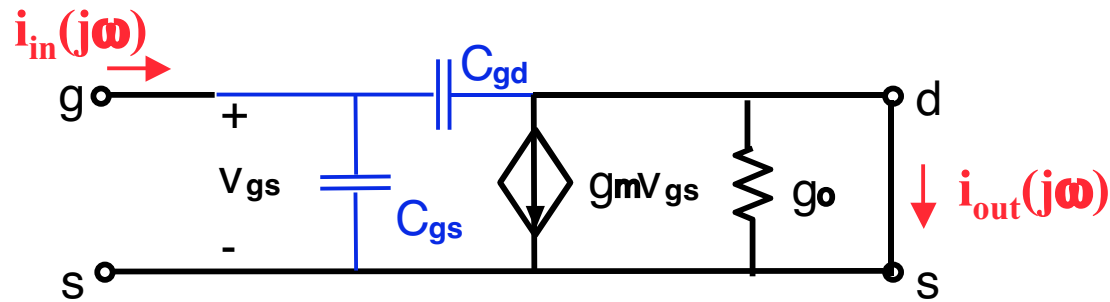
$$q_G = W q N_{Dn} \int_0^L x_d(y) dy \approx -W L q N_{Dn} \sqrt{2\epsilon_s (\phi_b - v_{GS})} / q N_{Dn}$$

$$\text{Thus, } C_{gs} \equiv \partial q_G / \partial v_{GS} \approx W L \sqrt{\epsilon_s q N_{Dn} / 2(\phi_b - v_{GS})}$$

We'll use this shortly.

High frequency models - short circuit current gain

A measure of the high frequency performance of a transistor is obtained by calculating its short circuit current gain, $\beta_{sc}(j\omega)$, and finding the frequency at which its magnitude is 1:



$$\beta_{sc}(j\omega) = \frac{i_{out}(j\omega)}{i_{in}(j\omega)} = \frac{j\omega C_{gd} v_{gs} - g_m v_{gs}}{j\omega(C_{gs} + C_{gd})v_{gs}} = \frac{j\omega(C_{gd}/g_m) - 1}{j\omega(C_{gs} + C_{gd})/g_m}$$

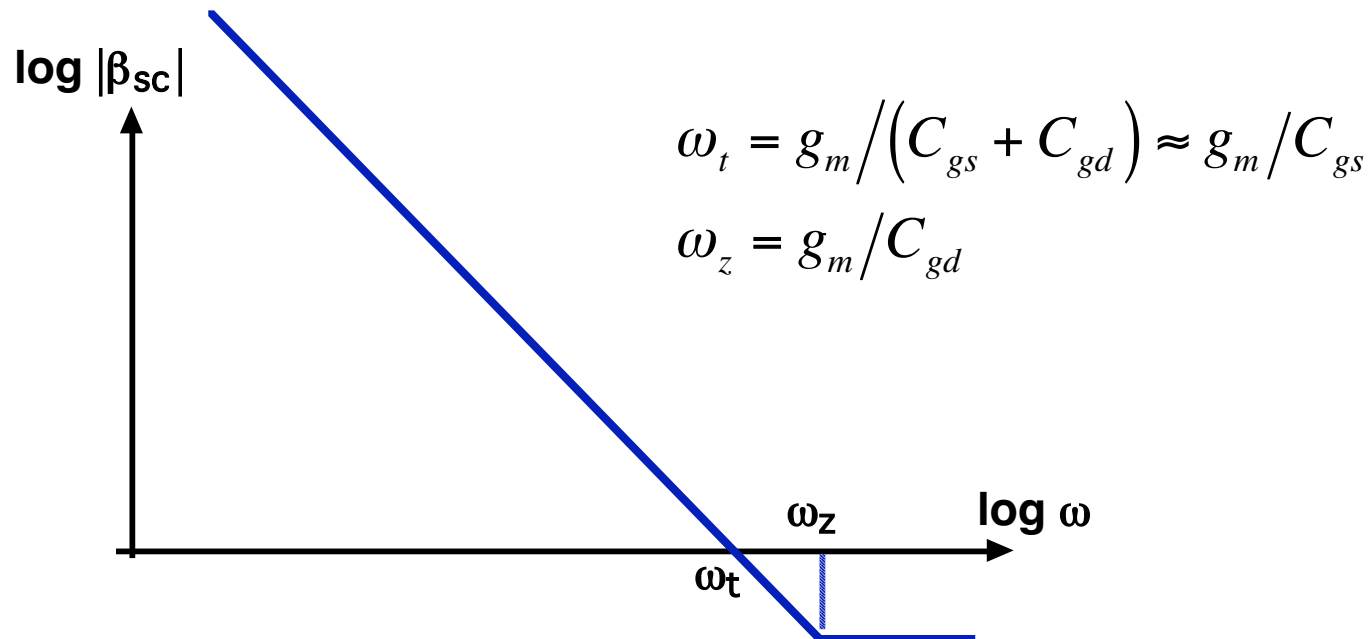
$$|\beta_{sc}(j\omega)| \approx \frac{g_m}{\omega(C_{gs} + C_{gd})} \quad \text{for } \omega \ll g_m/C_{gd}$$

$$\text{and thus, } |\beta_{sc}(j\omega)| = 1 \quad @ \quad \omega_t = g_m / (C_{gs} + C_{gd})$$

Note: $C_{gs} \gg C_{gd}$, so the assumption is valid, i.e., $\omega_t \ll g_m/C_{gd}$

High frequency models - f_t

A useful way to visualize this result is make a log-log plot of the magnitude of the short circuit current gain versus frequency, i.e., $\log |\beta_{sc}(j\omega)|$, vs. $\log \omega$. This is called a Bode plot:



Note: Usually $C_{gs} \gg C_{gd}$, so typically $\omega_z \gg \omega_t$.

High frequency models - The meaning of ω_t

We had:
$$\omega_t = g_m / (C_{gs} + C_{gd}) \approx g_m / C_{gs} \quad (\text{recall } C_{gs} \gg C_{gd})$$

Our model for a device with extreme velocity saturation gave us:

$$g_m = W s_{sat} \sqrt{\epsilon_s q N_{Dn} / 2 (\phi_b - v_{GS})}$$
$$C_{gs} = W L \sqrt{\epsilon_s q N_{Dn} / 2 (\phi_b - v_{GS})}$$

Thus:
$$\omega_t \approx s_{sat} / L$$

This can also be written as the inverse of some time, τ_{tr} :

$$\omega_t = 1/\tau_{tr}, \quad \text{where for this device } \tau_{tr} = L/s_{sat}$$

The time, τ_{tr} , is seen to be the transit time of the electrons through the channel. This is a very general result for ω_t , i.e., that it can be written as the inverse of the transit time of the relevant carriers through the device.

High frequency models - More on ω_t

The result,

$$\omega_t = 1/\tau_{tr}, \quad \text{where } \tau_{tr} = \text{device transit time}$$

is very general and very useful for evaluating a device concept. As examples of what might be found, we list below the results for MOSFETs and BJTs, along with the result we just obtained:

For an FET without velocity saturation:

$$\tau_{tr} = L^2 / \mu_e (V_{GS} - V_T)$$

For an FET with strong velocity saturation:

$$\tau_{tr} = L / v_{sat}$$

For an BJT without velocity saturation:

$$\tau_{tr} = W_B^2 / 2D_{\min.B}$$

One final model observation - Insight on g_m

We in general want an FET with as large a g_m as possible. We can get insight on how to achieve this by looking at our expression for ω_t , and using what we have learned about it being related to the transit time:

$$\omega_t = 1/\tau_{tr} \quad \text{and} \quad \omega_t = g_m / C_{gs}$$

Setting these two expressions for ω_t equal, and solving for g_m :

$$g_m = \frac{C_{gs}}{\tau_{tr}}$$

This result teaches us that to get a large g_m we must have:

1. The shortest possible transit time
2. The largest possible coupling between the gate electrode and the channel charge (that is, the largest possible C_{gs}).

MESFET Fabrication: A mushroom- or T-gate MESFET

(Image deleted)

See Hollis and Murphy in: Sze, S.M., ed. High Speed Semiconductor Devices,
New York: Wiley, 1990.

MESFET Fabrication - representative processing sequences

(Image deleted)

See Hollis and Murphy in: Sze, S.M., ed. High Speed Semiconductor Devices, New York: Wiley, 1990.

Double recess process

SAINT process

Microwave Monolithic Integrated Circuits: two views

Perspective view:

M-S Diode: 2 fF/cm^2 ,
 $1.6 \times 10^{-14} \text{ A}/\mu\text{m}^2$

FET: $I_{\text{DSS}} = 120 \text{ mA/mm}$,
 $V_p = -1.5 \text{ V}$, $f_T = 12.3 \text{ GHz}$,
 $g_m = 130 \text{ mS/mm}$ (all at
 $V_{\text{DS}} = 2.5 \text{ V}$, $V_{\text{GS}} = 0$)

R: 50Ω per sq.

C: 0.25 fF/cm^2

L: $1 \text{ nH}-20 \text{ nH}$

(Images deleted)

See Thayne, Elgaid, Terenent “*Devices and Fabrication technology [RFICs and MMICs]*” in *RFIC-and-MMIC-design-and-technology* ed. By I.D. Robertson and S. Lucyszyn (IEEE, London, UK 2001) pp. 31-81.

Top view:

Microwave Monolithic Integrated Circuits: an implanted mesa process

(Image deleted)

See Bahl, I. and Bhartia, P., Microwave Solid State Circuit Design
Hoboken, N.J., Wiley-Interscience, 2003.

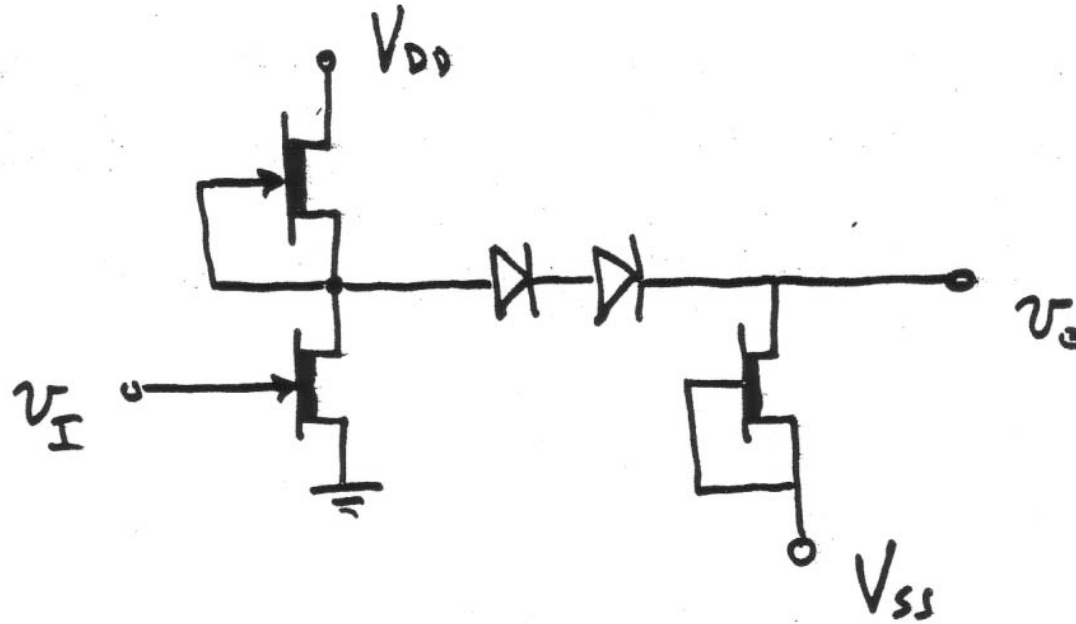
Microwave Monolithic Integrated Circuits: a planar implanted process

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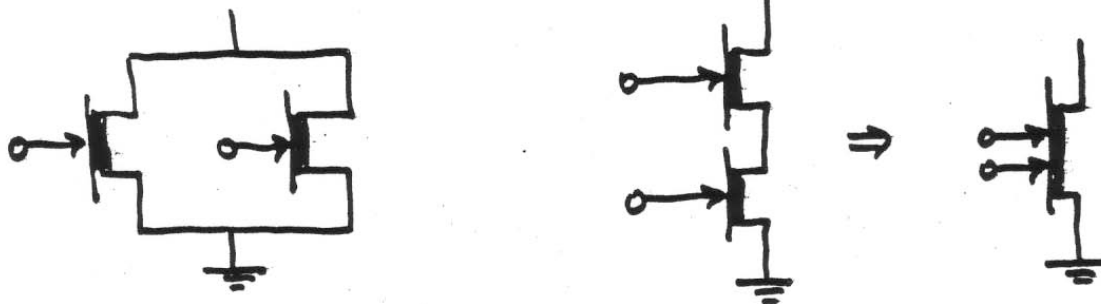
See H. Singh et al, IEEE 1991 Microwave and Millimeter-Wave Monolithic Circuits Symposium

MESFET Logic Families: FET Logic (FL)

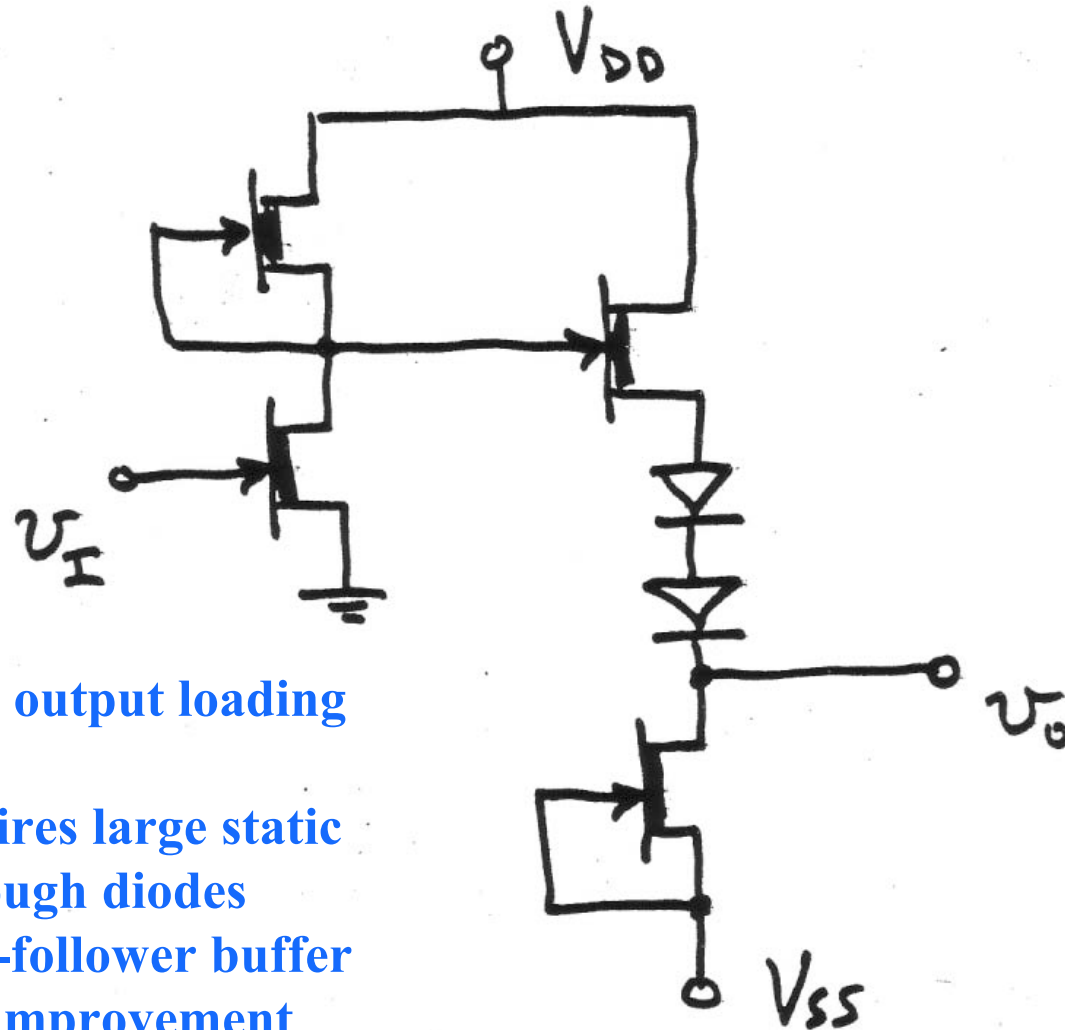
The challenge of normally-on logic:



Multiple inn....

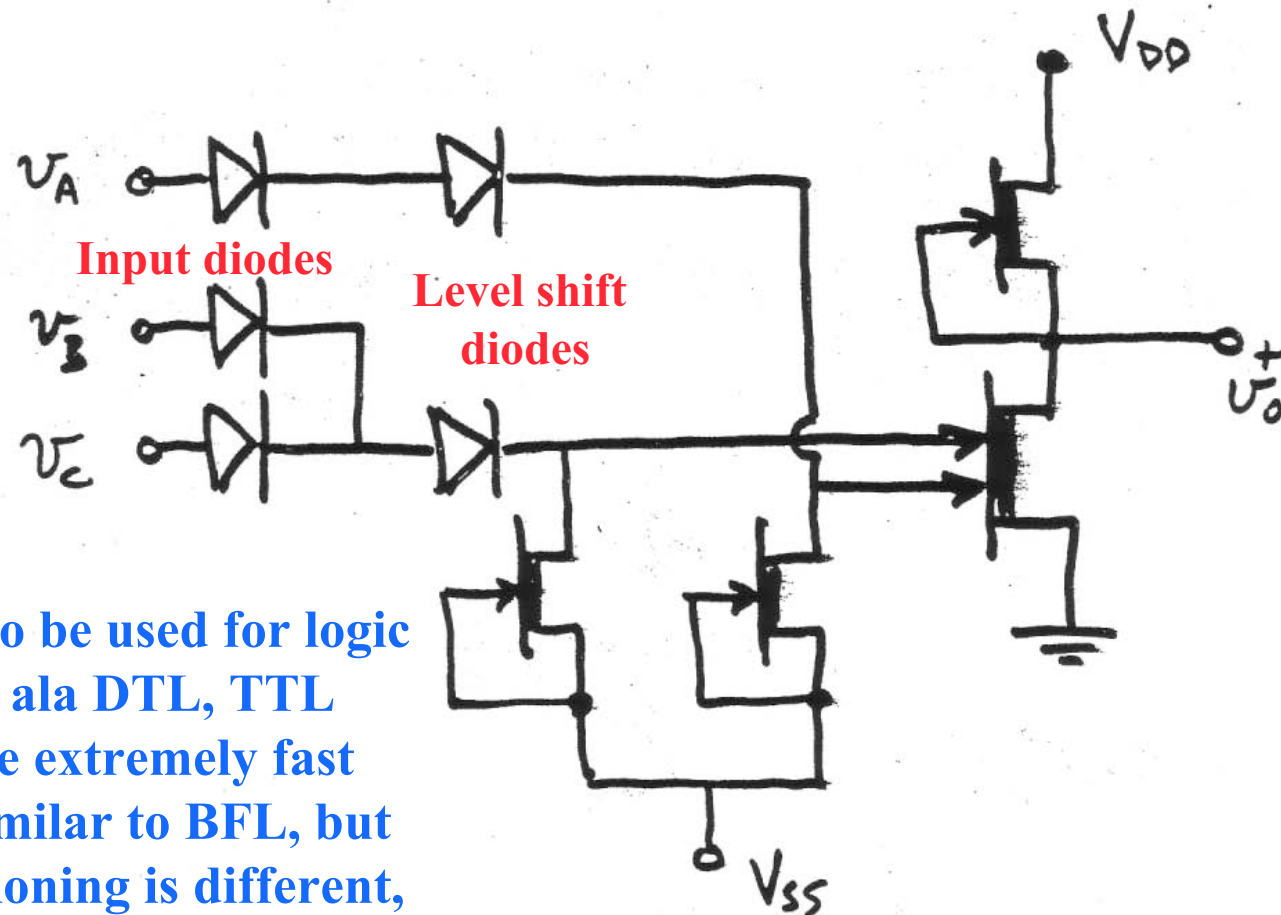


MESFET Logic Families: Buffered FET Logic (BFL)



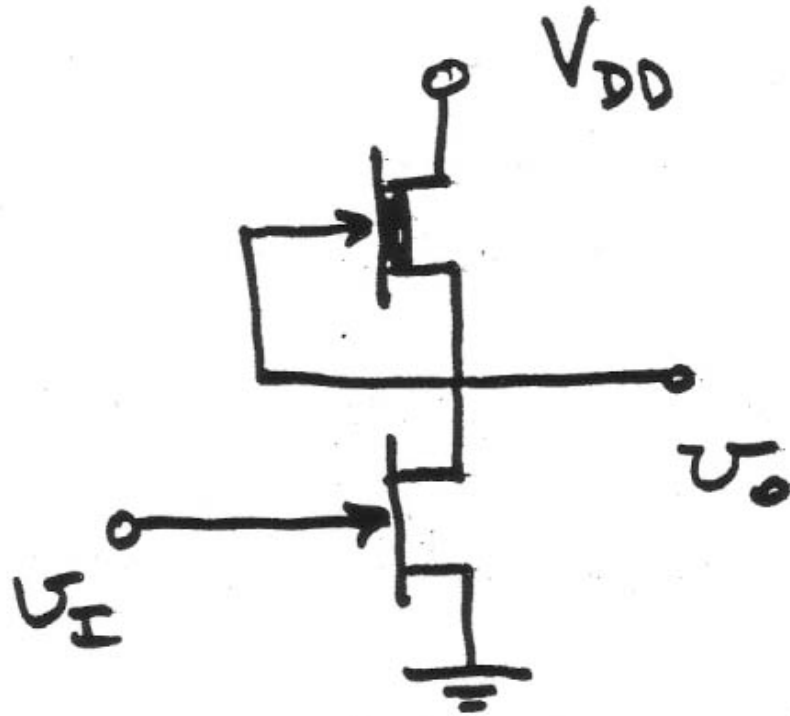
FL is effected by output loading
(fanout)
High speed requires large static
current through diodes
Adding a source-follower buffer
yields a big improvement

MESFET Logic Families: Schottky Diode FET Logic (SDFL)



Diodes can also be used for logic functions, ala DTL, TTL
M-S diodes are extremely fast
This is very similar to BFL, but the partitioning is different, and now multiple inputs are added by adding more diodes

MESFET Logic Families: Direct coupled FET logic (DCFL)



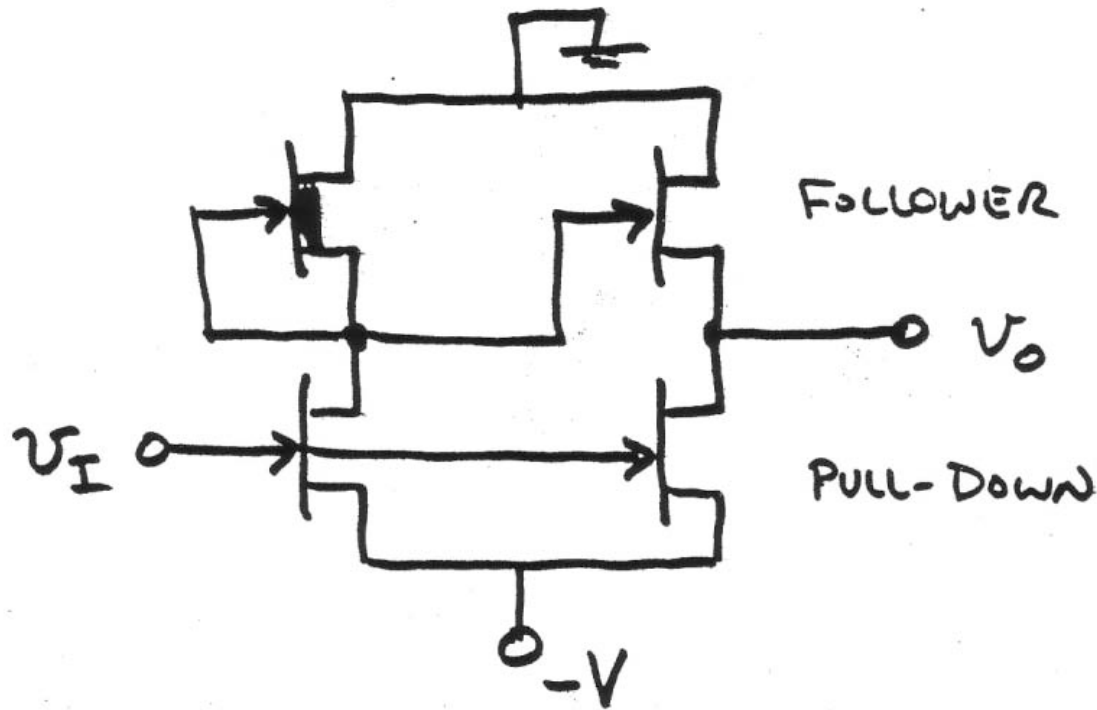
Requires both e-mode and d-mode devices

The MESFET equivalent of n-MOS

The input voltage must be less than the turn-on voltage of the gate

This circuit provides good speed, low power, and high density

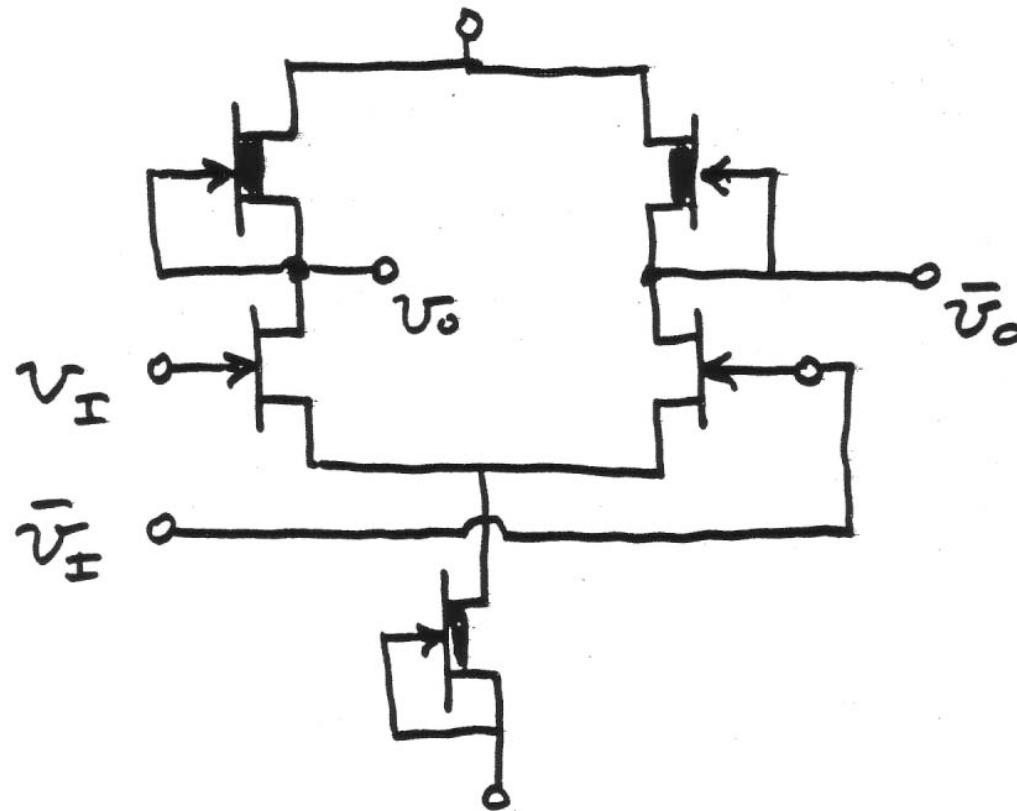
MESFET Logic Families: Super-buffer for DCFL (SBFL)



The switching performance of DCFL can be improved by using a quasi-complementary push-pull driver

Multiple inputs each require a switch and pull-down transistor
This circuit introduces some spiking on the lines so the supply and ground must be robust.

MESFET Logic Families: Source-coupled FET logic (SCFL) or Current mode logic (CML)

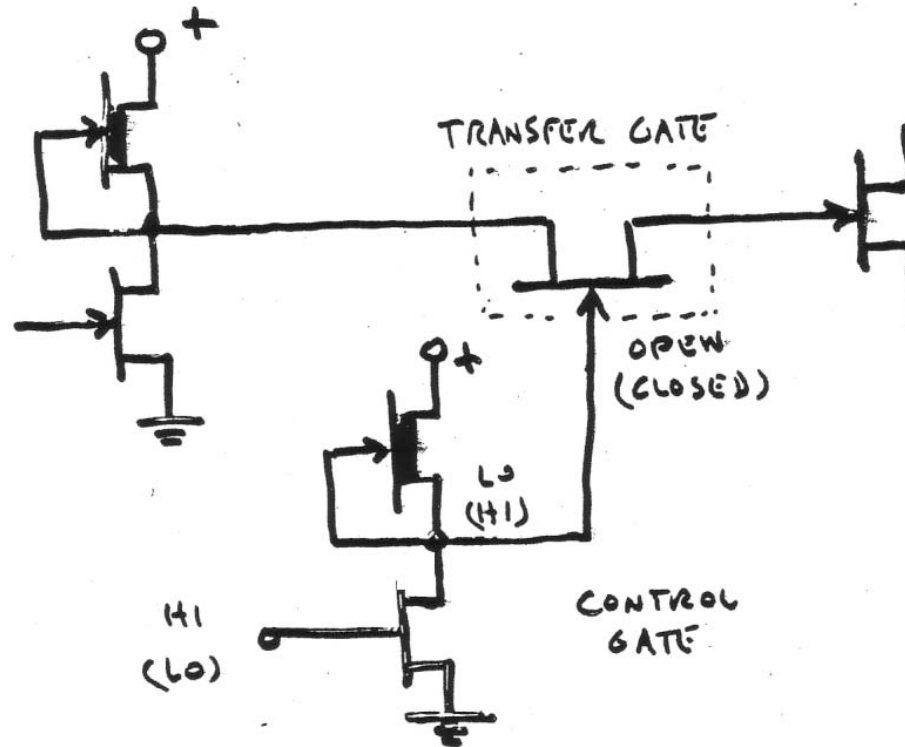


The MESFET equivalent of ECL

The output must be level-shifted before going to the next stage

Comparison of three MESFET logic families: layouts and logic swings

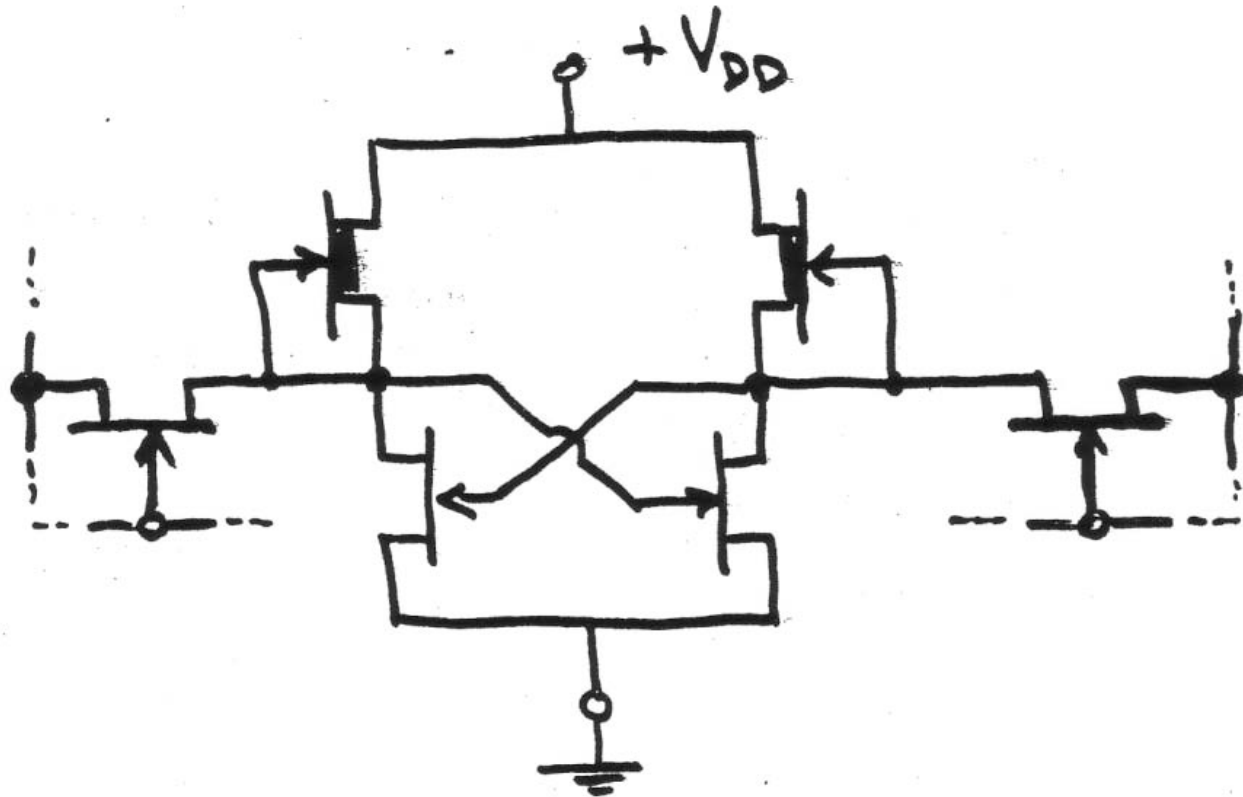
Transfer gate



A single FET connected in a pseudo-common-gate configuration functions as a transfer gate.

A normal logic gate is used to open and close the transfer gate

Memory cells



High gate leakage levels have precluded the successful use of dynamic memory cells with MESFETs.

All memory is based on static cells (flip-flop stages)