MASSACHUSETTS INSTITUTE OF TECHNOLOGY
Department of Electrical Engineering and Computer Science

6.374: Analysis and Design of Digital Integrated Circuits
Problem Set # 5

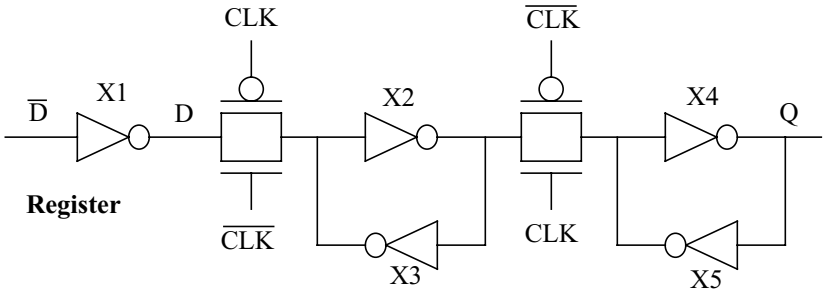
Fall 2003

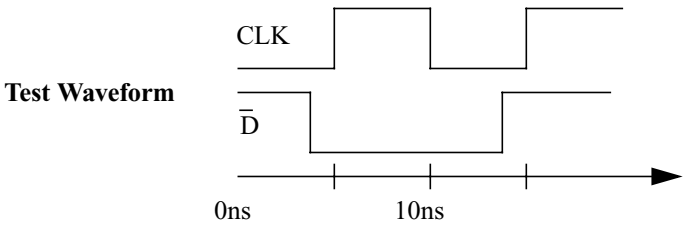
Issued: 10/28/03
Due: 11/12/03

For these problems you can use the process parameters for the 0.25 technology- see the Process Parameters file in the assignments section.

Problem 1: Transmission Gate Register Design

Having mastered the art of register and latch design you are faced with the following problem. Your manager asks you to design a "Reduced Clock Load Transmission Gate Register". You look up your 6.374 Bible, and Bingo! You have it right there in Handout #7, Slide 24. Good thing you took the class, at least you have the schematic to begin with :)





a) What type of register is this? Briefly explain how it works.

b) Your problem is to *size* the inverters and transmission gates. Assume a supply voltage of 2.5V and fully static inverters. Simulate the circuit in HSPICE with the input waveforms shown in the figure. Assume negligible rise and fall times for the CLK and $\overline{CLK}$ signals and no skew between them. To begin with assume all NMOS devices to be minimum sized and all PMOS devices to be 3 times the NMOS devices. Assume Q is 0V initially.
Does your circuit work? (There goes my raise!). Turn in plots showing input waveforms along with D and Q signals.

Resize the transistors so that the circuit is functional. Point out the changes you have made and explain clearly. Turn in the same plots as in (b) but simulated with modified sizes.

Hint: Do not HSPICE the circuit to death. It would be better if you used .SUBCKT macros and tweaked only those sizes that you think will matter. Think before you simulate!

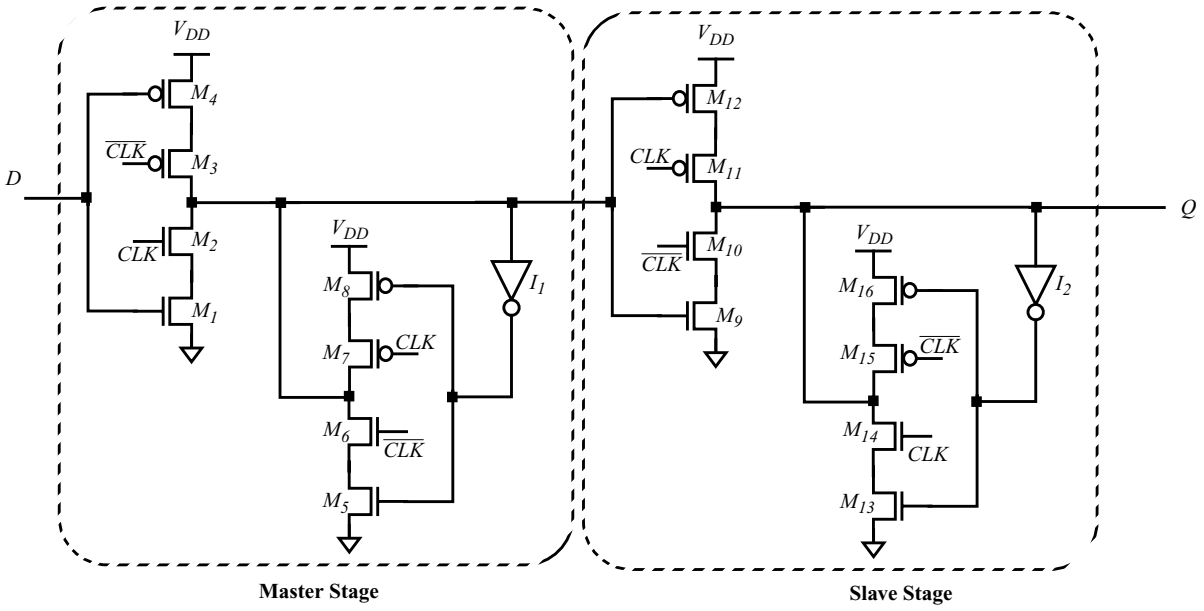
Problem 2: Edge Triggered Register

Consider the following edge-triggered register. Assume that the clock inputs *CLK* and $\overline{CLK}$ have a 0V to V_{DD} swing. Also assume (for parts a-c) that there is no skew between *CLK* and $\overline{CLK}$ (i.e., the inverter delay to derive $\overline{CLK}$ from *CLK* is zero). Assume that the rise/fall times on all signals are zero.

a) What type of register is this? (Positive Edge-Triggered Register or Negative Edge-Triggered Register). Explain.

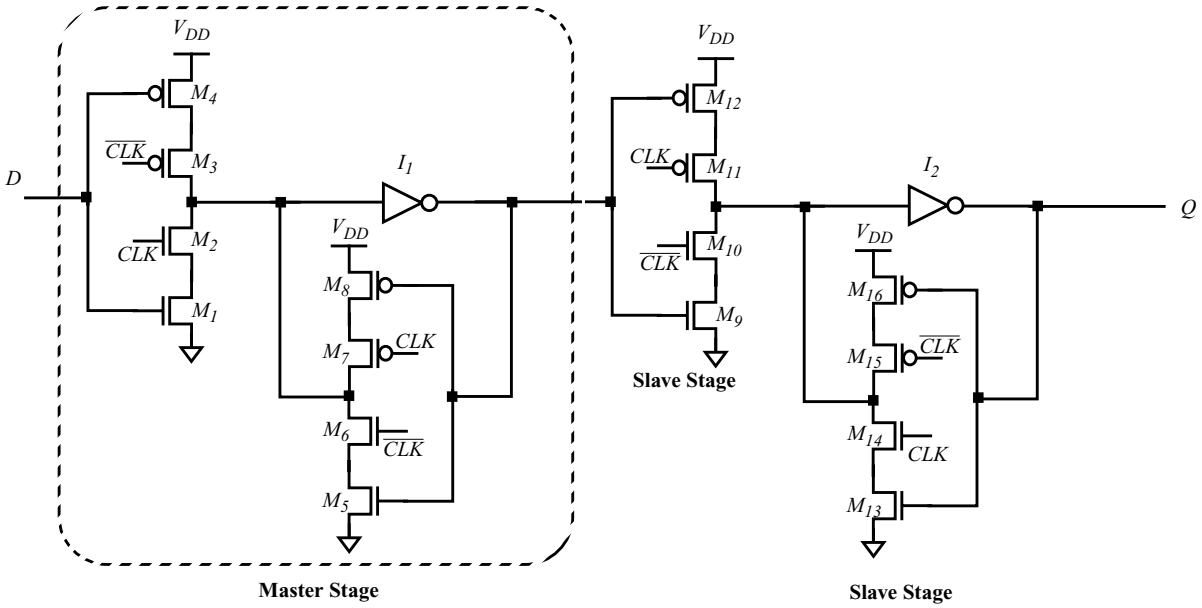
b) Assume that the propagation delay of each clocked inverter (e.g., M_1-M_4) is T_{CK_INV} and the delay of inverters I_1 and I_2 is T_{INV}. Derive the expression for the set-up time (t_{su}), the propagation delay ($t_{c\text{-}q}$) and the hold time (t_h) in terms of the above parameters. Explain your results.

c) What is the function of transistors M_5-M_8 and M_{13}-M_{16}? Is this circuit Ratioed?



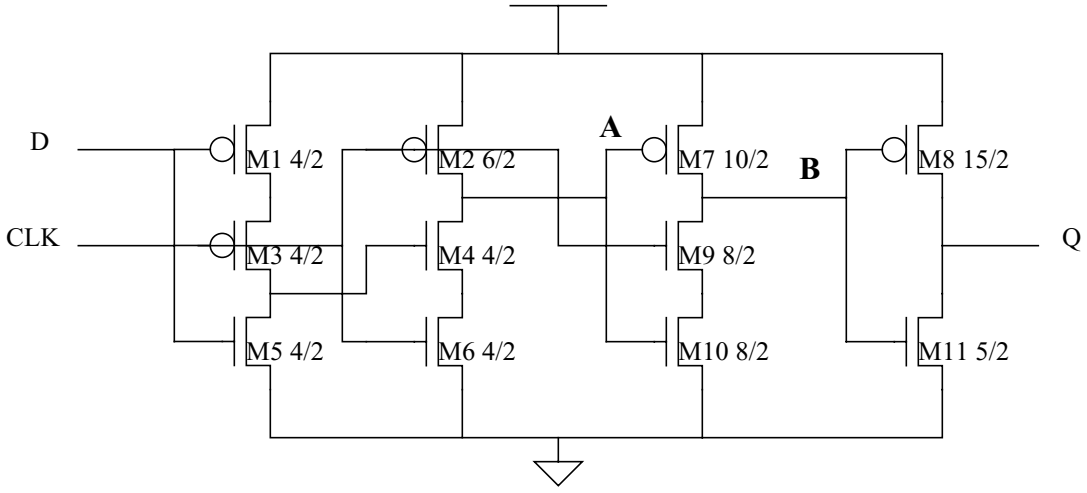
d) Consider the following variation of the circuitin the figure below. If there is a clock overlap, is there a potential problem? If so explain the problem and describe the condition when it happens.

.



Problem 3: True Single Phase Flip-Flop.

Consider the True Single Phase Flip-Flop shown here:



Simulate the circuit in HSPICE. The sizes of the devices are given in terms of lamda. Make sure you initialize node B and that you use stimuli given below.

.ic nB=pvdd
*nb is the node noted B on the schematic

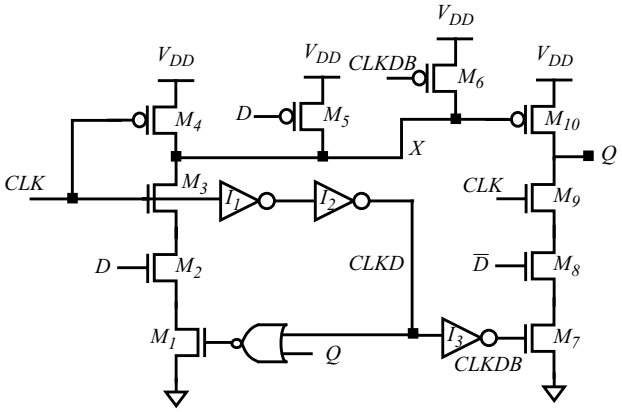
Vclk clk 0 pulse (0 pvdd 10n 0.5n 0.5n 10n 20n)
Vd d 0 pwl(0n 0v 25n 0v 25.5n pvdd 45n pvdd 45.5n 0)

Do you see the glitching at the output? Explain what happens. Change the sizes of 2 transistors and fix the glitch-

ing. Turn in a table with the new sizes and a spice plot showing the new glitch-free flip-flop output. For the corrected flip-flop, measure the setup time using HSPICE and report it in the table as well. **As a reminder:** AS=AD= W (in µm) x 0.625 µm, PS=PD= W (in µm) + 1.5µm

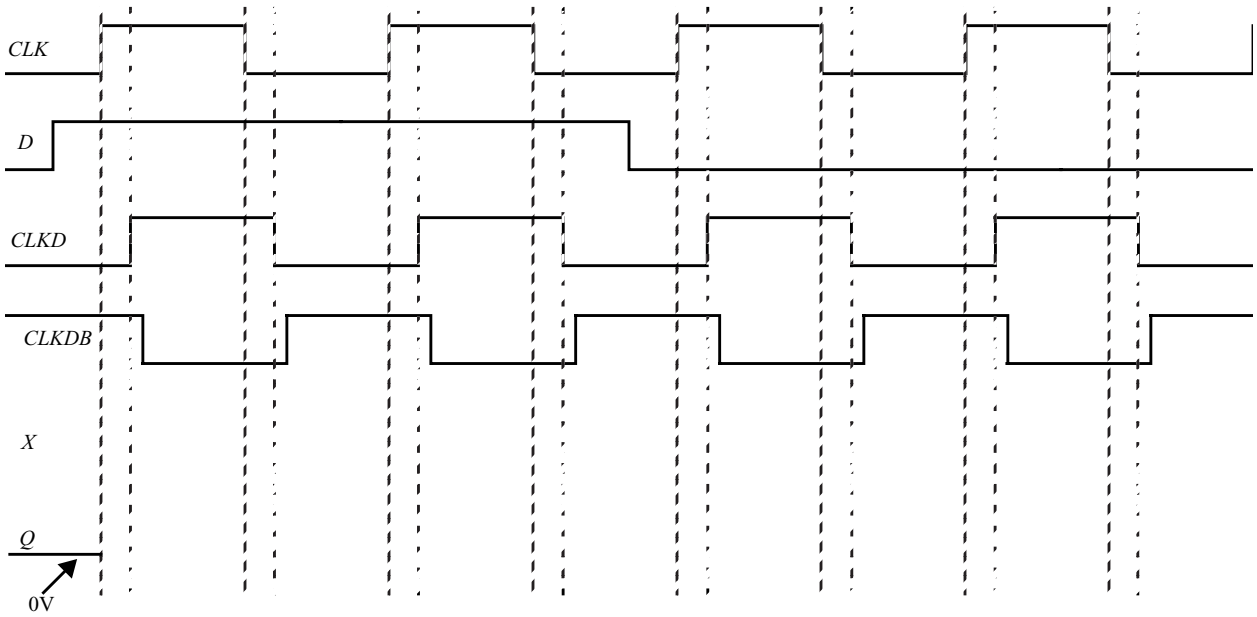
Problem 4: Sequential Circuit

Consider the following sequential circuit. Assume that there is no delay between D and $\overline{D}$ (i.e., the inverter delay to obtain $\overline{D}$ from D is 0). Assume that the output is statically held using circuits not shown here (i.e., ignore leakage effects for this problem). Assume that the rise/fall times on all signals are zero.



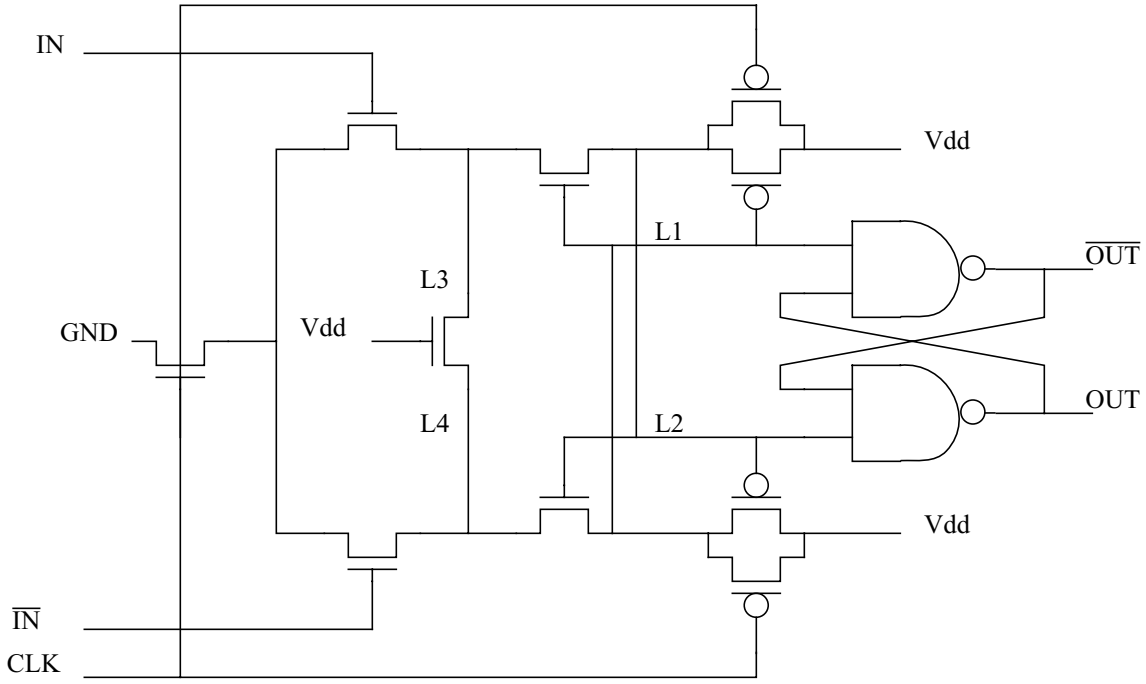
a) Complete the following timing diagram for X and Q.

Assume that the inverter delay is much smaller than the clock period and that appropriate set-up/hold times are met. Assume that each gate (I_1, I_2, I_3, NOR, M_1-M_4 and M_7-M_{10}) takes 1 time unit for a low to high or high to low transition. Also assume that it takes 1 time unit to charge node X through M_5 or M_6. Both the propagation and contamination (i.e., minimum) delay are equal to 1.



b) What is the set-up time for this circuit if glitches on the output Q are acceptable? Explain.

Problem 5: DEC StrongARM Low Power Edge-Triggered Flip-Flop



The flip-flop shown in the above figure is used in the StrongARM microprocessor developed by Digital Equipment Corporation for the Portable Electronic Device (PED) market. Note that it is fully differential. The following questions will help you understand the operation of this flip-flop. No calculations are necessary for this problem.

a) When clock is low is the flop holding or is it transparent? Why? (2 sentences)

b) What is the purpose of the shorting transistor connecting nodes L3, L4? (2 sentences)

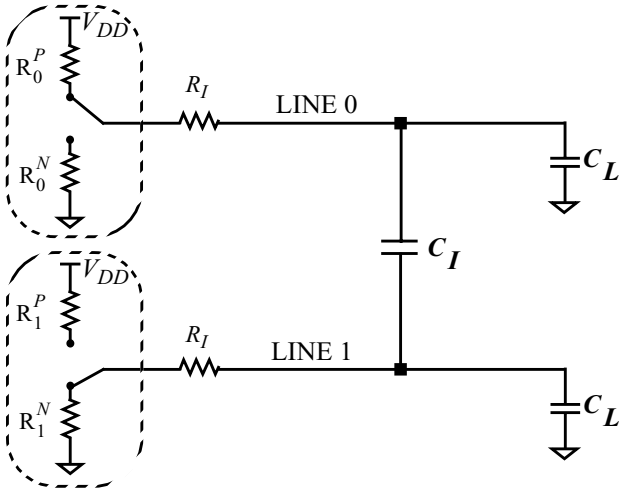
c) What is the main advantage of this flip-flop from a low power perspective? (1 sentence)

d) What determines the setup time for this flip-flop? Draw a timing diagram showing the timing relationship between the data and the clock. (1 sentence)

e) From a system perspective, where should this flip-flop be used (i.e., in datapaths for pipelining, as receivers at the end of long buses, as state bits for FSMs,etc.)? Why?(1 sentence)

Problem 6: Submicron Interconnect Effects.

Consider the following interconnect circuit. C_L is the lumped capacitance of each line to ground and C_I is the inter-wire capacitance. The driver (inverter) is modeled using resistors and an ideal switch. The Switch is ideal and is connected either to the top resistor or the bottom resistor. R_I is the effective resistance of the interconnect. For this problem, let $\lambda = \frac{C_I}{C_L}$.



(a) Assume that the initial voltage on line *i* (where *i* = 0 or 1) is V_i^{OLD} and the final value after all the transients have settled is V_i^{NEW}. $V_i^{OLD}, V_i^{NEW} \in \{0, V_{DD}\}$. Derive an expression for the energy drawn from V_{DD} through *driver 0* for an arbitrary transition of the two bit bus.

b) Assume that $\lambda = 0$ for this part. The total energy (i.e., including both drivers) drawn from the power supply for a sequence can be written as $\eta \bullet C_L \bullet V_{DD}^2$. Estimate the value of η for the following two sequences.

Sequence A: $00 \rightarrow 01 \rightarrow 11 \rightarrow 10$

Sequence B: $00 \rightarrow 11 \rightarrow 00 \rightarrow 11$

c) Assume that $\lambda = 3$ for this part. The total energy (i.e., including both drivers) drawn from the power supply for a sequence can be written as $\eta \bullet C_L \bullet V_{DD}^2$. Estimate the value of η for the following two sequences.

Sequence A: $00 \rightarrow 01 \rightarrow 11 \rightarrow 10$

Sequence B: $00 \rightarrow 11 \rightarrow 00 \rightarrow 11$

d) For the transition of the bus from 01 to 10, compute the total energy dissipated in the resistors.

Problem 7: Data-Dependent Logic Swing Internal Bus Architecture (DDL Bus)[1]

Consider the DDL bus architecture for an N bit bus. (Refer to the figures in the lecture notes.)

a) Assuming M bits switched to 0, by what factor do we save power compared to the conventional full swing bus? (remember that there are always 2 bits switching to 0 to provide the “0” and ”1” references)

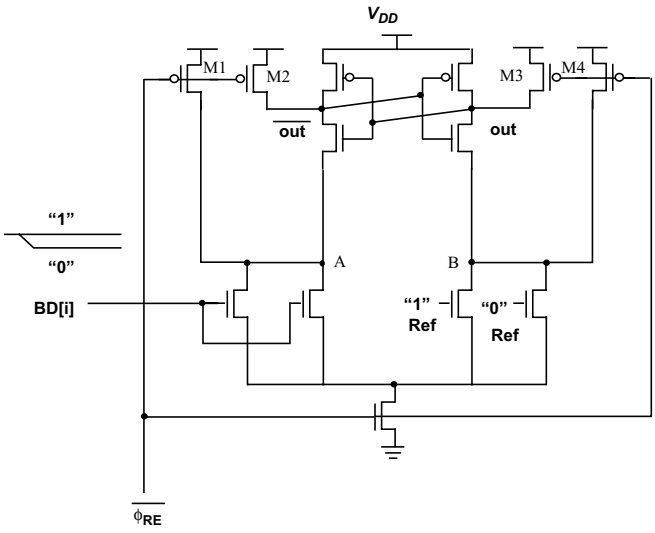
b) What is the range of “0” ref? Why are there two “0” refs ?

c) What is the reason for having M2 and M3? Wouldn’t it be enough just to have M1 and M4 charge up the nodes A and B to turn the inverter off during precharge?

The following figure shows the receiver for the DDL bus architecture. (Dual Reference Sense Amplifying

1.M. Hiraki, H. Kojima, H.Misawa, T. Akazawa, Y. Hatano, “Data-Dependent Logic Swing Internal Bus Architecture for Ultralow-Power LSI’s”, IEEE Journal of Solid State Circuits, vol.30, no.4, April 1995 pp. 397-402

Receiver)



Dual reference sense amplifying receiver.