MASSACHUSETTS INSTITUTE OF TECHNOLOGY

Department of Electrical Engineering and Computer Science

6.301 Solid State Circuits

Final Exam

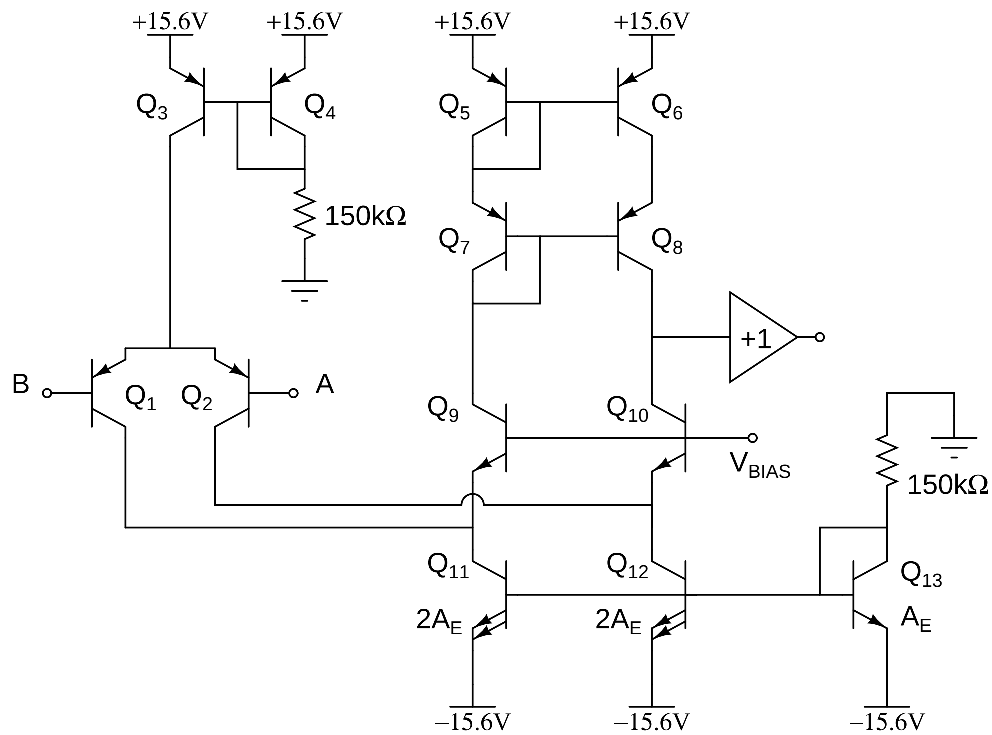
December 20, 2006

180 minutes

1. This examination consists of four problems. Work all problems.
2. This examination is closed book.
3. Please summarize your solutions in the spaces provide in this examination packet. Draw all sketches neatly and clearly where requested. Remember to label ALL important features of any sketches.
4. All problems have equal weight.
5. Make sure that your name is on this packet and on each examination booklet.

Good luck.

Problem 1



(a) Which input terminal, A or B, is the inverting input?

(b) Assuming all base currents are negligible, and that $V_{BE,on} = 0.6\text{V}$, determine the collector currents for all 13 transistors.

(c) A classmate approaches you trying to determine the bandwidth of this circuit. He is complaining that the OCTC analysis is taking forever, because there are so many devices.

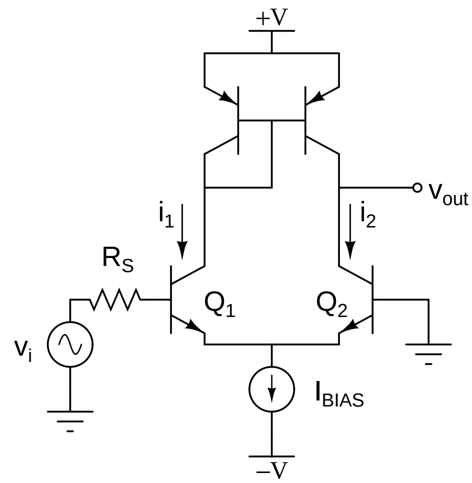
In a single, short paragraph, argue that:

(1) There are only a couple of devices that need careful attention.

(2) In this case, the OCTC estimate will be very good.

Problem 2

Consider the following amplifier:

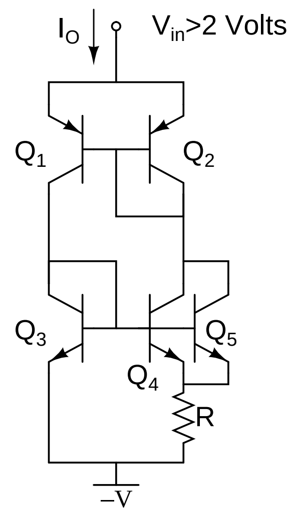


(a) Fill out the following table (reproduced on the answer sheet), indicating if the small-signal circuit parameter increases (+), decreases (-), or stays the same (0) in magnitude for an increase in R_S, I_{bias}, V_A, and T. Assume that all transistors are matched and have the same V_A, β, etc., that R_S and β_0 are independent of I_{bias} and T; and that c_μ is constant. Do not ignore the Early effect.

Points will be deducted for incorrect answers. (It is better to leave a block blank than to guess randomly.)

	$R_S \uparrow$	$I_{\text{bias}} \uparrow$	$V_A \uparrow$	$T \uparrow$
midband gain a_{vd}				
output resistance R_o				
Upper 3db frequency ω_h				
CMRR				

(b) In practice, we cannot use an ideal current source to bias the transistor. Consider the following non-ideal current source:



Assuming R is independent of temperature, write I_o in terms of R, k, T, and q. Assume that the Early voltage for those devices is infinite, and that they have infinite β and equal values for I_S. While this circuit can have $I_o = 0$, assume this is not the case.

If we replace I_{BIAS} in the circuit in part (a) with this new current source, what is the new effect of an increase in temperature on the midband gain (+/-/0)?

Problem 3

The included figure shows 8 operational-amplifier connections. You may assume that the amplifiers have ideal characteristics. Determine which of the connections can provide each of the following relationships between v_O and v_I.

(a) $v_O = 4v_I$

(b) $v_O = -v_I, \quad v_I > 0$

$v_O = 0, \quad v_I < 0$

(c) $v_O = -K_1 \ln \frac{v_I}{K_2}$

K_1 and K_2 are (possibly temperature dependent) scale factors.

(d) $\frac{v_O}{v_I} = \frac{1}{s^2/\omega_n^2 + 2\xi s/\omega_n + 1}$

(e) $v_O = v_I$

(f) $v_O = v_I, \quad v_I > 0$

$v_O = 0, \quad v_I < 0$

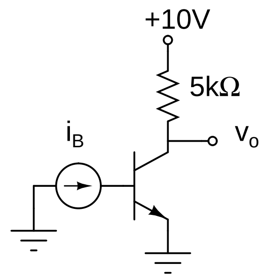
(g) $v_O = +10\text{V}, \quad v_I > 5\text{V}$

$v_O = -10\text{V}, \quad v_I < -5\text{V}$

v_O is indeterminable, $-5 < v_I < +5$

(h) $\frac{v_O}{v_I} = \frac{s^2/\omega_n^2}{s^2/\omega_n^2 + 2\xi s/\omega_n + 1}$

Problem 4



When the transistor is in its forward active region,

$$i_C = \frac{q_F}{\tau_F}$$
$$i_B = \frac{q_F}{\tau_{BF}} + \frac{dq_F}{dt}$$

When it is in saturation,

$$i_B - i_{B0} = \frac{q_s}{\tau_s} + \frac{dq_s}{dt}$$

The charge control parameters for this transistor are:

$$\tau_F = 1\text{ns} \quad \beta_F = 100 \quad \tau_{BF} = 100\text{ns}$$
$$\tau_R = 2\text{ns} \quad \beta_R = 5 \quad \tau_{BR} = 10\text{ns}$$
$$\tau_S = 15\text{ns}$$

For parts (a) and (d) that follow, assume that $e^{-t/\tau} \approx 1 - \frac{t}{\tau}$. Express the answer to part (c) in terms of a log.

The base current is a step of 1mA.

(a) The voltage v_O starts at +10 Volts and approaches 0 Volts. Determine the time it takes for v_O to reach +5 volts.

(b) Determine the steady state value of q_S, assuming $v_{CE(\text{SAT})} \approx 0$V.

(c) After steady state is reached, the base current is stepped to zero. The output voltage eventually reaches 10 Volts. How long does it take for v_O to reach +5 volts?

(d) In order to speed up return to $v_O = +5$ volts, the base current is stepped to $-I$ rather than 0. What value of I is required so that the return of v_O to +5 volts is the same as the time found in part (a)?

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