Massachusetts Institute of Technology
Department of Electrical Engineering and Computer Science

6.111 - Introductory Digital Systems Laboratory

Brief Introduction to the HP Logic Analyzer

There are two principal instruments used by digital engineers to test and debug digital systems. The oscilloscope is used in order to make accurate timing measurements and to investigate voltage vs. time characteristics of signals. Oscilloscopes generally have a limited number of channels. Logic analyzers have many more channels, have limited timing resolution, and display only binary signals. In the 6.111 lab we have instruments which combine logic analyzers and digital oscilloscopes. The Model 1663AS has 32 logic analyzer channels, the Model 1662AS has 64 channels. Both have two `scope channels. These logic analyzers can be configured as timing analyzers which give a waveform display similar to that of an oscilloscope or as state analyzers which display signals in terms of binary or hex numbers, or both at the same time.

The logic analyzer is a fairly complex instrument. There are numerous documents provided by HP to explain its use. At the instrument room desk you may sign out a Training Kit, containing a signal source card and a Guide with a series of tutorial lessons on how to use the instrument. At several places in the laboratory there is a three-ring notebook containing the full-fledged Reference Manual. All of this documentation, including this document, are best read in the laboratory while you are seated in front of the logic analyzer so that you can try out various operations as they are described.

The logic analyzers are set up and controlled by interacting with menus. It will be much easier for you to learn the operation of the analyzer by trying out menu selection as you go along. Indeed, you can learn a considerable amount about the logic analyzer without even hooking up any signals to the logic analyzer. Turn on the logic analyzer and wait for it to complete its internal diagnostics and load the initial configuration. The logic analyzer has a disk drive that can be used to store configuration files. You will find it desirable to have your own 3.5" DSDD (1.0 MB) disk, which is available at the instrument room.

Front Panel Controls

The front panel consists of a display, disc drive, menu buttons, key pad, and cursor knob. There is also a mouse which can be used for most control operations. The cursor knob is used for scrolling through ranges of fields or for adjusting time per point, delay, etc. The mouse, with its buttons, can be used (largely interchangeably) with the ``Menu,'' directional arrow buttons, ``Select'' and ``Done'' buttons to select operations.

Preparing Your Own Disc

From the power-on state, click on ``Analyzer'' and select ``System,'' then click on ``RS-

232/HP-IB" and select ``Disk." Click on ``Load" and select ``Format Disk." To proceed to formatting a disk, insert a BLANK disk in the drive, click on ``Execute" and ``Continue."

Now you can ``Store" any configuration you want to save to your disk and at some later time ``Load" it back into the analyzer.

There does not seem to be any simple way to initialize the logic analyzer to its power-on state. However, if you store this state into a file on your disc, then you can get back to the power-on state at any time by loading the stored file. Go to the I/O menu and select disc operations. Select the left-hand field and then select the store operation. Now enter a name, such as INITIAL_LD, as the destination file name and execute this operation. Now you can reset the logic analyzer to the initial condition by loading the file INITIAL_LD from disc.

Selecting Menus

The system configuration screen is one of several menus. The others are easily selectable by the mouse. To get back to the system configuration file from one of the other menus, select the upper one-in-from-left field of one of these menus and then select the desired menu. Actually the format, trigger, and display menus consist of a menu for each enabled analyzer. In the system menu the initial condition is that analyzer 1 is selected to be a timing analyzer and analyzer 2 is off. Change Analyzer 2 to be a state analyzer. Now select the configuration menu, and you can get either state format specification for machine 2 or timing format specification for machine 1. You can move between these easily using the mouse.

System Menu

Two separate analyzers can be configured. Each can be either off, a timing analyzer, or a state analyzer. The system menu is also used to assign pods to analyzer 1 or analyzer 2. Each pod has its own cable to a connector on the back of the analyzer and provides sixteen channels plus a clock. Each channel is indicated by a dash or an up-down arrow. The up-down arrow indicates that transitions on that signal are occurring.

Format Menu

The primary use of the format menu is to enter labels and assign individual signal(s) to those labels. You can turn a label on or off or modify it, which means that you can enter new text for that label. In this menu you can also select a threshold which is used to determine whether the pod signal is 1 or 0. Almost all of the time you will keep the default threshold set for TTL. When in the state format menu you can also select the clock which will be used to sample the pod signals for each state. There is one clock signal for each pod. They are labeled J, K, L, and M for pods 1 through 4 respectively. You can enable the sampling of data on the falling, rising , or both edges of the clock, or when it is low or high. If you select multiple clocks, then the state will be sampled when either of the selected conditions is satisfied. You can even select clocks which are wired to pods which are not assigned to this state analyzer. If you have both analyzers as state analyzers you can use one clock to clock the lower eight bits and another to clock the upper eight bits. Details are given in Chapter 11 of the Reference Manual.

Trigger Menu

As with the format menu, there are two types: the timing trigger specification and the state trigger specification. The basic function of both of these menus is to decide what information to store and when to stop storing information and switch to the display menu. Both of these menus can be set to capture a single set of data or to repetitively capture and display data. The term ``to arm'' means that when the arm condition has occurred, the analyzer starts looking for the trigger condition. Most of the time, the arming is accomplished by pushing the run button. Sometimes an analyzer may be armed by the other analyzer. The method of specifying the trigger condition is different for timing and state analyzers. A timing analyzer triggers after encountering a selected pattern and then a selected edge of one or more signals. You can specify a constraint that the specified pattern must be present for > some time period or < some time period. If you have selected that the pattern be present for >, then you can trigger on an edge. The edge trigger can be falling, rising, or either edge of one or more signals. If you set the base to binary, then the normal display clearly shows which edges cause the trigger. If you set the base to hex, then you will see a $ sign to indicate that some trigger is specified for that hex digit. If you have selected <, then the logic analyzer triggers whenever the specified pattern has existed for less than the specified time period. If you set the acquisition mode to glitch and select >, then you can specify the trigger to occur on the OR of edges or a glitch. A glitch is any transition crossing the logic threshold more than once between samples. The logic analyzer is not guaranteed to detect glitches which are less than 5 ns wide. In glitch acquisition mode, the amount of data that can be stored is reduced, as half the memory is used for storing the data samples and the other half for storing the second transition of a glitch in a sample.

State Trigger Menu

The state trigger menu is organized somewhat differently but serves the same function of specifying when the logic analyzer is to trigger. It also specifies the states that are to be stored before and after triggering. Rather complicated sequences can be specified. When the state analyzer is used to debug software running on a microprocessor or a microsequencer, the logic analyzer can be set to look for the nth entry to a particular subroutine and then the nth entry of a subroutine called within that subroutine. This can be continued for up to eight levels.

A complete description of the state trigger specification menu is given in chapter 12 of the Reference Manual.

Display Menus

The display can be of waveforms or listings for either type of logic analyzer selected. In the waveform display, you can set the time/div and the trigger; and the display looks much like a multi-trace oscilloscope. If you select the markers field, you can turn them Off or turn them to indicate Time. You then can control the position of the X and O markers, and the time difference between these markers and between the markers and the trigger will be displayed.

In the listing display, the sample number is displayed in the left-hand column with the sampled signals in the remaining columns. You can use the knob to scroll this information up or down. You can also move to any position by entering the number of the data sample. If you wish, you can use the markers and have them placed on specified patterns for easy identification of events. For more information on use of the markers, see pages 13-4 through 13-11 and 14-12 through 14-20 in the Reference Manual.

You can switch the type of analyzer between state and timing without changing anything else and re-acquire the data if you wish to go between waveform and state displays. If you have two analyzers enabled, one as a timing analyzer and one as a state analyzer, there is a third mixed mode display which allows you to see both timing and state information.

Printed January 14, 2002