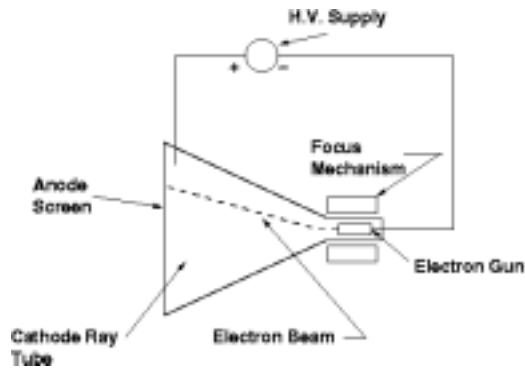**Vido Displays are usuall implemented by Cathode Ray Tubes**

Electron Beam os focused into a small spot on the screen

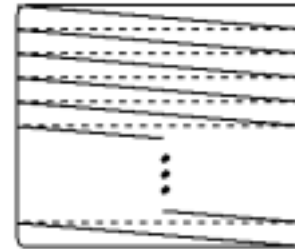**Energy delivered to a phosphor creates a glowing dot (pixel)**

Beam can be moved rapidly in 2 dimensions

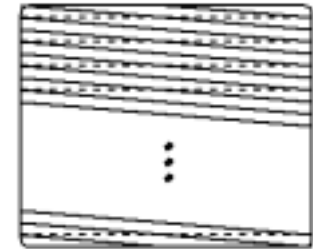**Beam current determines brightness of the spot**

1

Video Diaplays

Television and most computer displays use raster-scan:

Non–Interlaced: Frame rate may be 60, 72, etc. frames/sec

———— Scan line

- - - - - - Retrace line

Interlaced. Frames alternate This is like Television: 60 half frames/sec.

2

Composite Frames

The 'frame' is a single picture (snapshot)
It is made up of many lines
Each frame has a synchronizing pulse (Vertical Sync)
Each line has a synchronizing pulse (Horizonatl Sync)
Brightness is represented by positive voltage
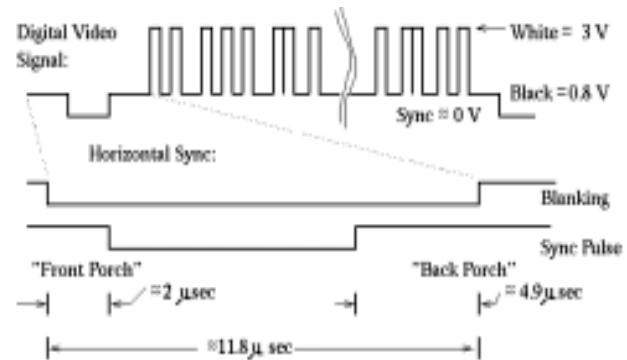**Horizontal and Vertical intervals both have blanking**
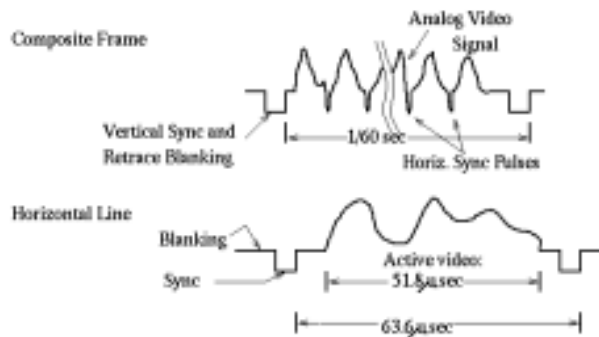
3

Digital Displays

White Dots on a Black Screen
White is positive
Black is a low voltage
Sync is below black

Sync pulse is in the middle of the blanking interval

4

Composite Synchronization

Horizontal Sync coordinates lines
Vertical Sync coordinates frames
Similar but for time scales
  And they are superimposed on one another
These numbers are for television like displays

Recovery of Signals

Composite Video has picture data and both syncs
  Video is above sync level
  Separation is easy
Sync recovered by noting when composite is below sync level
  Horizontal sync is used directly
  Vertical sync is slower:
    Low pass filter
    Square up with Schmitt Trigger

Generation of Signals

Assume 1 bit per pixel
This is a simple way of building a front end
  Timing about right for TV style displays
  's38 is fast open collector part

Control

Try this display format:
  256 pixels X 192 rows
  7.16 MHz clock ==> .13966 microseconds/pixel
  Display time = 35.8 microseconds (active line)
  256 X 192 = 49,152 = 48k pixels = 6k bytes

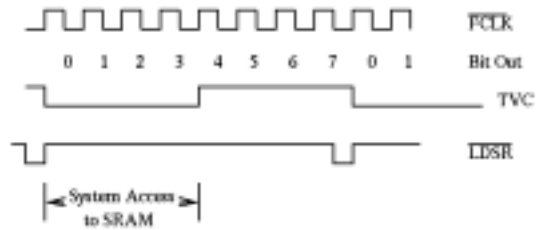**This control scheme would work:**

Timing of Control Signals

    Frame Counters and ROM produce sync signals
        FCLK is at pixel rate
        SCLK is FCLK/4
    TVC controls picture memory access
    LDSR controls loading shift register
    DLD controls system access to picture memory

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Generation of Sync Signals, etc.
    These are just bits in ROMs
    Note that EOL (active low) causes a line count and clears dot counter
    And that (EOF AND EOL) causes a clear of line counter

H: Bits 7:0 are high bits of memory address
L: Bits 5:1 are low bits of memory address

10
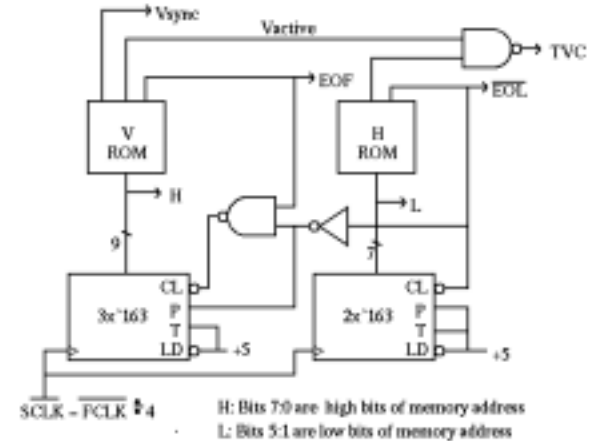
What would go into those ROMs

Vertical PROM:

Number of Locations	Addresses	Bits Set
192	0 - 191	Vactive
26	192 - 217	Vblanking
6	218 - 223	Vsync
37	224 - 260	Vblanking
1	261	EOF

Horizontal PROM:

32	0 - 31	Hactive
9	32 - 40	Hblanking
7	41 - 47	Hsync
8	48 - 55	Hblanking
1	56	EOL

11

Color Displays

    Are similar to 3 black and white
        Colors Add
        Here is the schedule for an "8 Color Display"
        More colors possible with more bits

    Sync is often carried separately
        Sometimes is on the Green line

|	R	G	B
Black	0	0	0
Blue	0	0	1
Green	0	1	0
Cyan	0	1	1
Red	1	0	0
Purple	1	0	1
Yellow	1	1	0
White	1	1	1

12

Character Displays

    Characters are fixed bit patterns
        Have the same shape
        Can appear at different places on the screen
    Letters and numbers are characters
        But other patterns can be useful
    On a 256 column X 192 row screen:

Char Size	Rows	Columns	Chars/Page	
8 x 16	12	32	384	(16 X 12 = 192)
8 x 12	16	32	512	

    Use of Characters can save video memory: 256 X 192 = 49152 dots
                                        = 6144 bytes
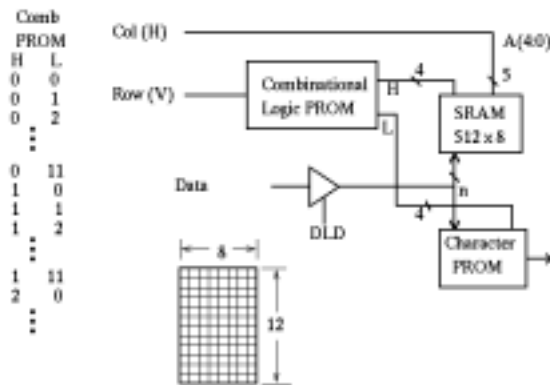
Character Format (8 x 16 pixels)

    Simple Formatting:
        Lower 4 bits of screen address
        indicate which row in character
        9 bits of screen address tell which character
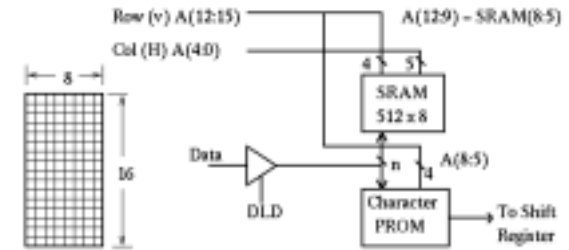
Character Format (8 x 12 pixels)

    Row formatting not quite as simple
        But re-mapping is done easily in a PROM

Video Controllers

    MC6847 is obsolete but easy to use
        Several display modes
        256 x 192 2 color (well, 1 and black)
        Other color graphics with lower resolution