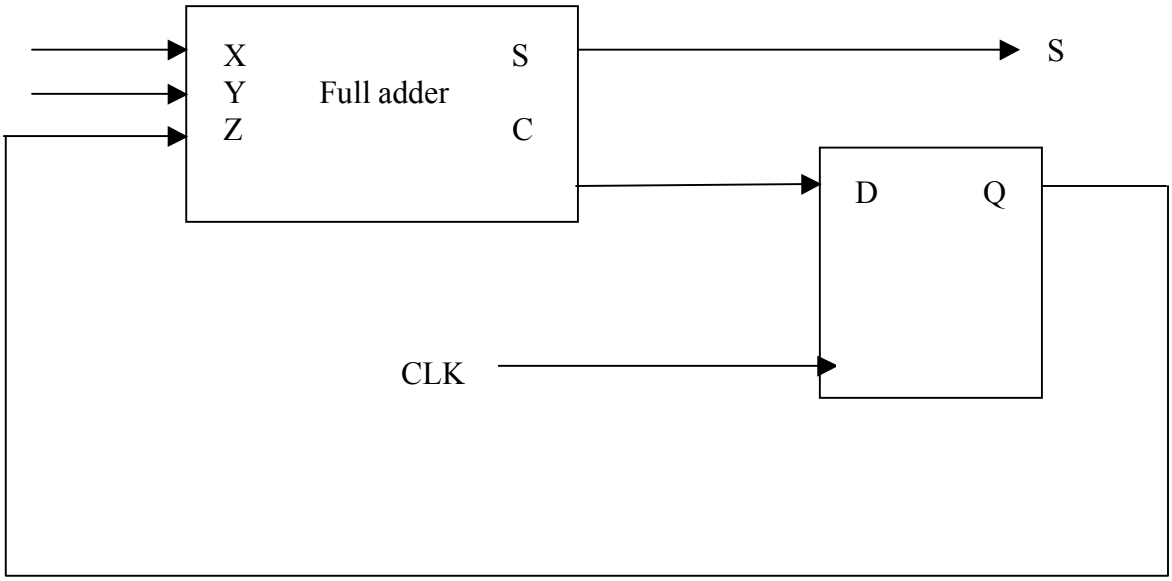
Massachusetts Institute of Technology
Department of Electrical Engineering and Computer Science
6.111 – Introductory Digital Systems Laboratory

Problem Set 4 — Lecture 10 Day
Due: Lecture 12 Day

Problem 1: Simple Finite State Machine

The sequential circuit below has one D flip-flop, two inputs (X and Y), and one output (S). The circuit consists of a full adder circuit whose carry output is connected to a D flip-flop.



1. Derive the truth table for the above circuit.
2. Draw the state diagram for this circuit (be sure to show the output S in the diagram).
3. Is the finite state machine of the Moore type or the Mealy type? Explain.
4. Assume that the timing characteristics for the flip-flop are $t_p = t_{setup} = t_{hold} = 2$ μs, and for the full adder $t_p = 4$ μs. Assuming that all inputs (X and Y) are synchronous with the system clock, what is the greatest clock speed at which the system could run?

Problem 2: Parking Ticket Machine

At Back Bay garage, Don and Larry are thinking of using an automated parking ticket machine to control the number of guest cars that a member can bring. The card reader

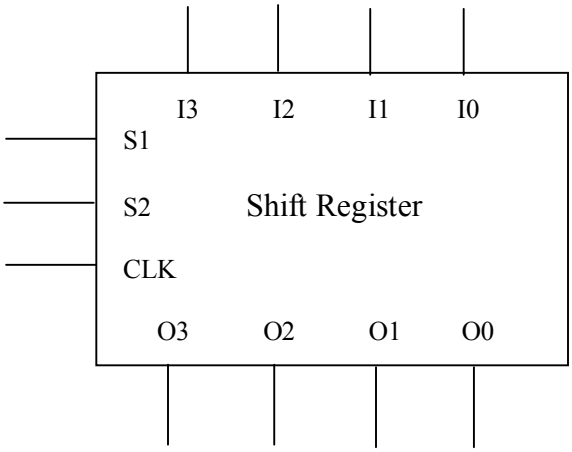
tells the controller whether the car is a member or a guest car. Only one guest car is allowed per member at a discount rate only when s/he follows out the member at the exit (within the allotted time). The second guest must pay the regular parking fees. You have been hired to implement the control system for the machine which is located at the exit. Using your expertise on FSMs, design the control system.

- Signals from the card reader: MEMBER and GUEST
- Signals from the toll booth: TOKEN (meaning one toke received),
- EXP (time for discounted guest payment has expired).
- Signal to the gate: OPEN.

Fee: Members are free, Guest w a Member is 1 Token, Regular Guest is 2 Tokens.

1. Draw a truth table that corresponds to the FSM.
2. Draw the equivalent Karnaugh map.
3. Turn in your state diagram, carefully labeled. Be sure to indicate which state the FSM is in after a RESET.
4. Is this a Moore or Mealy machine?

Problem 3: VHDL Code for Bi-Directional Shift Register



S1	S0	Operation
0	0	Hold Preset Value
0	1	Shift Left
1	0	Shift Right
1	1	Parallel Load

The circuit shown above is a 4-bit bi-directional circular shit register with parallel load. The adjacent truth table indicates the operation state based upon the two select lines. The inputs are labeled I3, I2, I1, and I0. The outputs are labeled O3, O2, O1, and O0. This device is a circular shift register. This means that when shifting left, bit 3 is shifted onto bit 0, and when shifting right bit 0 is shifted onto bit 3.

Implement this device using VHDL. Confirm that your code compiles correctly with the device set to 22V10. Use the NOVA simulator to confirm that your code works correctly. Turn in a listing of your code and include a printout or sketch of a portion of your simulation.