6.012 - Microelectronic Devices and Circuits

Lecture 25 - Beyond Si; Beyond 6.012 - Outline

- **Announcements**
  - **HKN Evaluation - Do before final so you're still in a good mood.**
  - **Final - Tuesday, Dec 15, 9:00 am to Noon**
    - **Covering all the course; closed book; 4 problems**
- **Sub-threshold Circuit - What, Why, How**
  - **Applications:** medical implants, remote sensors, portable devices
  - **Digital design:** choosing V_{DD} for minimum energy per operation
- **Devices we have known - Where are they now:**
  - **MOSFETs:** 5 nm Si, III-V high electron mobility transistors
  - **BJTs:** InP based double heterojunction bipolar transistors
  - **LEDs:** white lighting; laser diodes
  - **Solar cells:** multi-junction, multi-material concentrator cells
- **Life after 6.012**
  - **Is it possible? (**"Where does one head after taking the header?"**)**

Sub-threshold Circuit Design: The need for low energy

Emerging applications require ultra-low energy:

Images removed due to copyright restrictions:
cartoons and figures illustrating microsensors, medical devices, ambient intelligence, and portable devices.

μ-sensors, medical devices

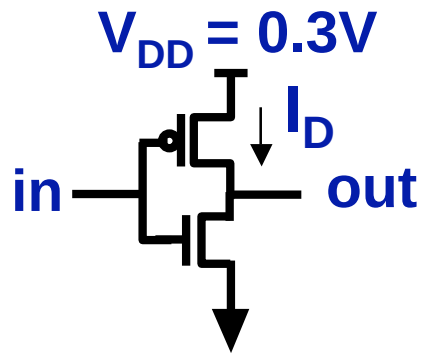
Ambient intelligence, portable devices

Sub-threshold operation:
Slow, lower power, minimum energy operation becomes possible

Sub-V_T benefits:
Power
Energy

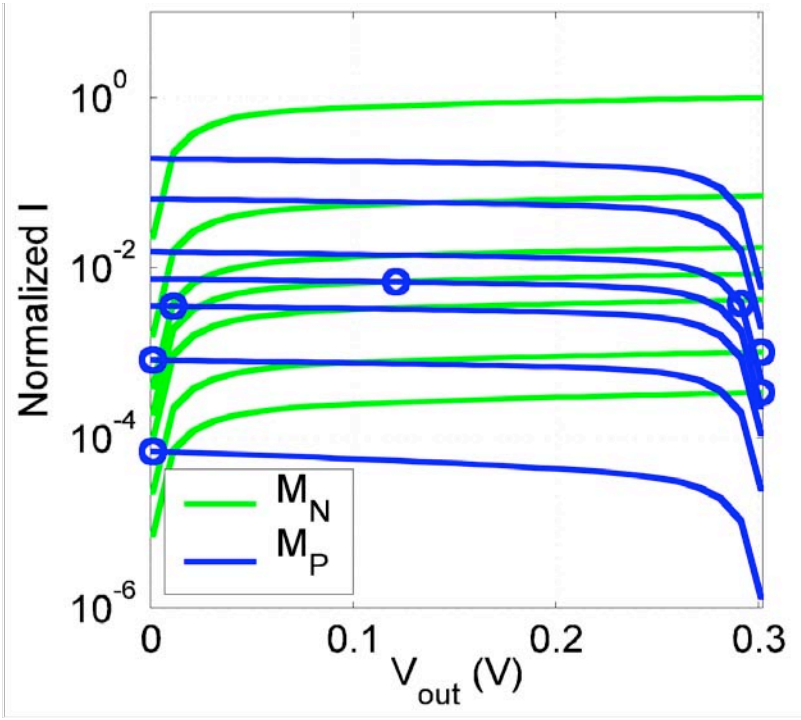
Concerns:
Increased sensitivity to noise and to variations in V_T and T.

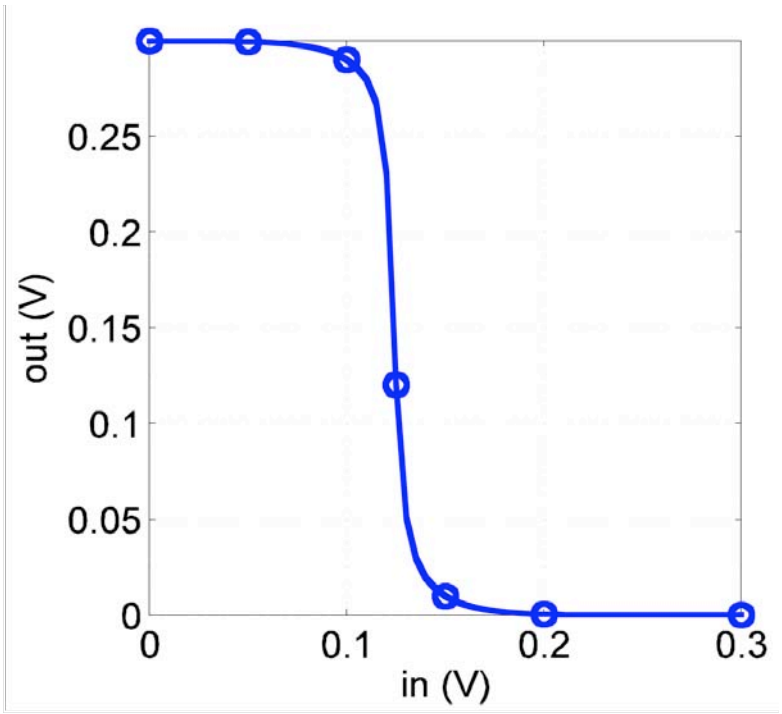
Sub-threshold Circuit Design: Digital Inverters, cont.



$$I_D = I_{S,s-t} e^{\frac{v_{GS}-V_T}{nV_t}} \left(1 - e^{-\frac{v_{DS}}{V_t}}\right)$$

with $$I_{S,s-t} = K V_t^2 (n-1)$$



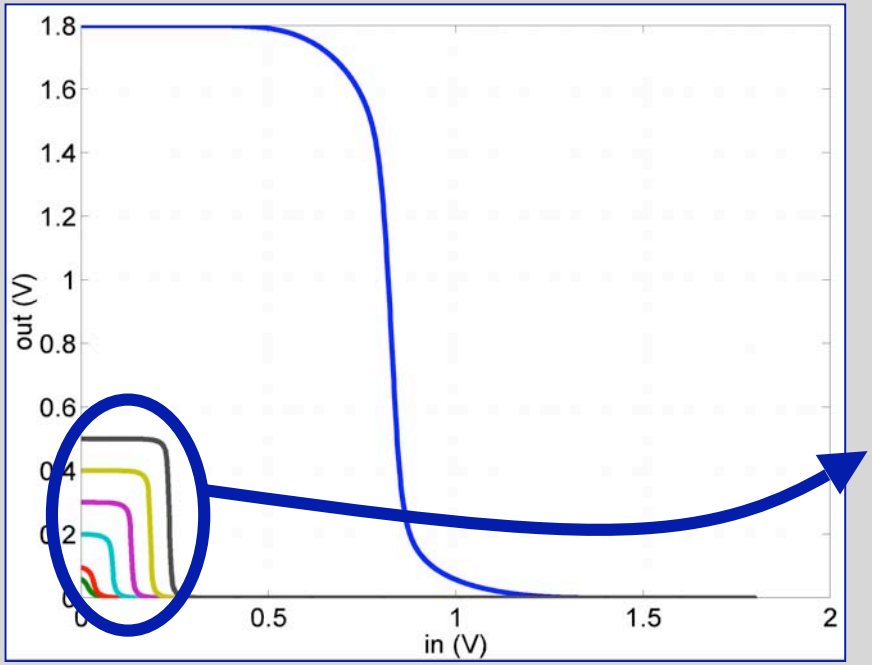


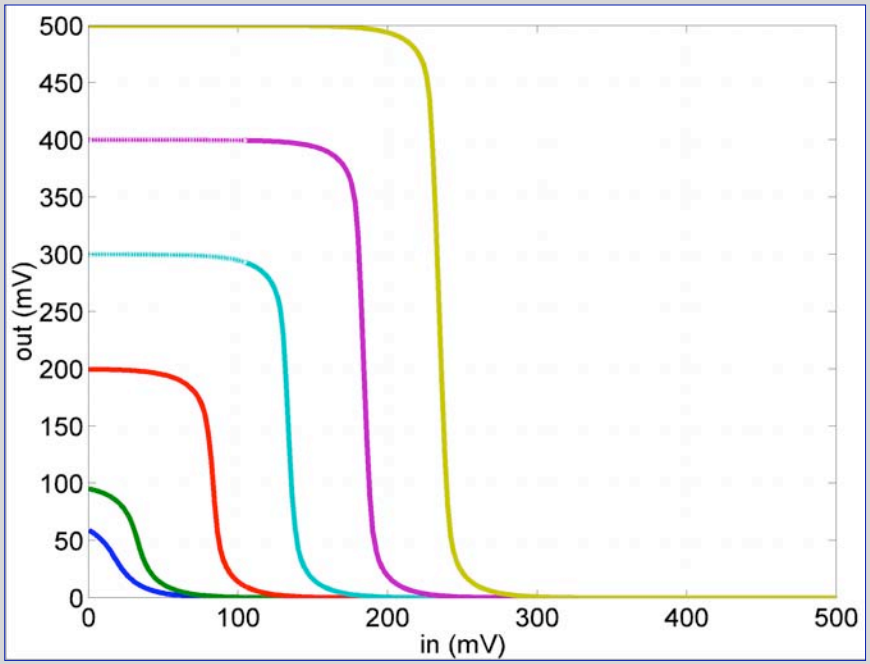
Work of Benton H. Calhoun at M.I.T. under Prof. Anantha Chandrakasan's supervision.

Sub-threshold Circuit Design: Digital Inverters

Operation of standard CMOS gate with $V_{DD} < V_T$

CMOS Inverter Voltage Transfer Curves $|V_T| = 0.5$ V





Work of Benton H. Calhoun at M.I.T. under Prof. Anantha Chandrakasan's supervision.

Sub-threshold Circuit Design: CMOS Inverters, cont.

In low-power applications an important metric the energy per operation, E_{pop}. There is an optimum supply voltage that minimizes E_{pop}.

Operating in strong inversion, $E_{pop} = C_L V_{DD}^2$, and reducing V_{DD} clearly reduces E_{pop}. As V_{DD} approaches V_T, however, the contribution of sub-threshold leakage becomes important, especially because the gate delay, τ_{GD} (time per operation) increases as charging current decreases.

In general:

$$\tau_{GD} = 2 C_L V_{DD} / I_{D,sat}$$

Only $I_{D,sat}$ is different depending on the region of operation.

In strong inversion:

$$I_{D,sat} = K\left(V_{DD} - V_T\right)^2 / 2$$

Sub-threshold:

$$I_{D,sat} = K V_t^2 (n-1) e^{(V_{DD} - V_T)/nV_t}$$

Just above threshold:

$$I_{D,sat} = K\left[V_t^2 (n-1) + \left(V_{DD} - V_T\right)^2 / 2\right]$$

Thanks to Naveen Verma for discussions on sub-threshold circuits.

Sub-threshold Circuit Design: CMOS Inverters, cont.

The energy per operation, E_{pop}, including energy dissipated by the sub-threshold leakage current, $I_{leakage}$ x τ_{GD} x # of idle gates is:

$$E_{pop} = C_L V_{DD}^2 + A I_{leakage} V_{DD} \tau_{GD} = C_L V_{DD}^2 \left[1 + 2A I_{leakage} / I_{D,sat}\right]$$

A is the average number of idle gates per active gate, and the leakage current is:

$$I_{leakage} = K V_t^2 (n-1) e^{-V_T / nV_t}$$

Evaluating E_{pop} in each region of operation we find:

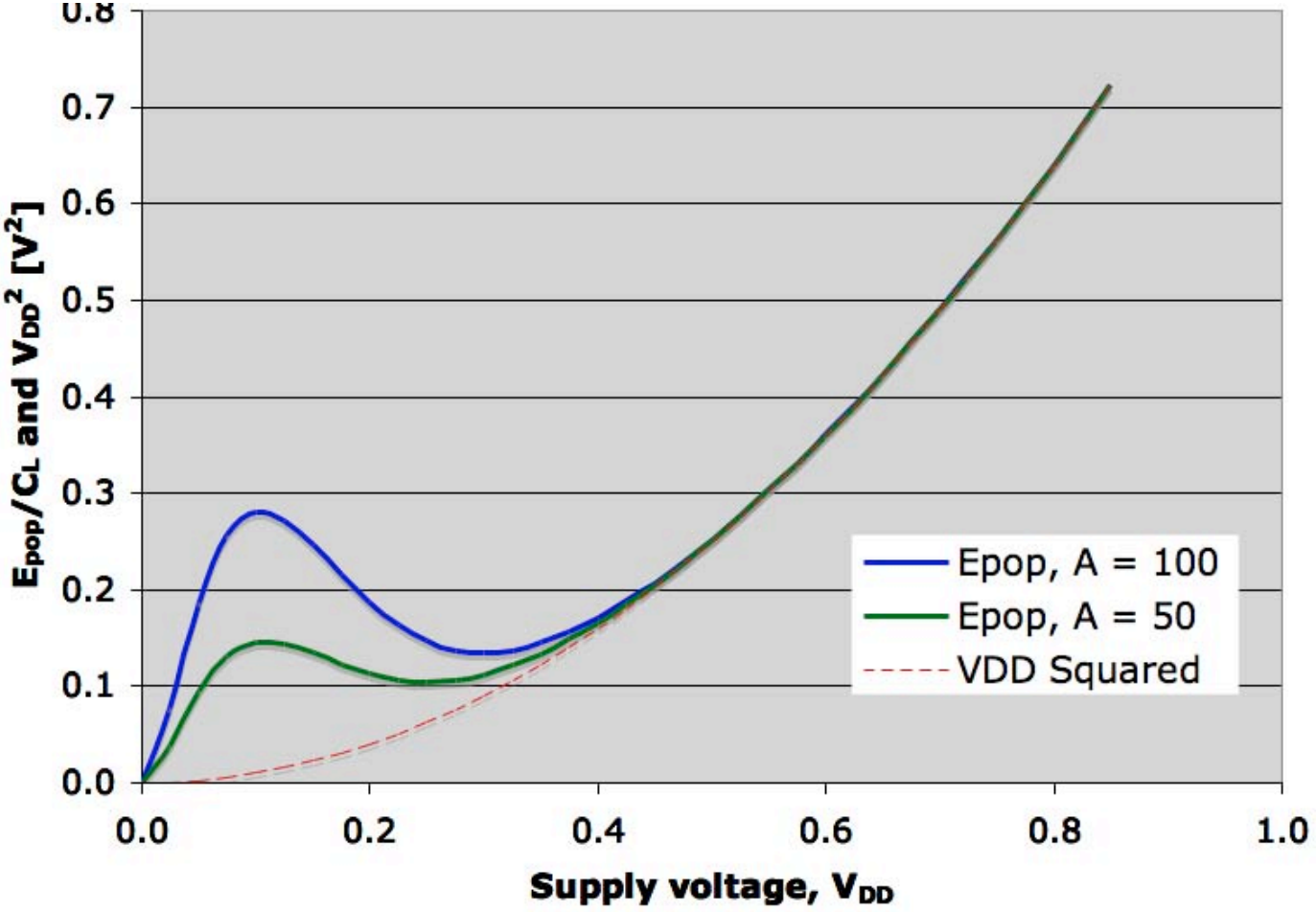
$$E_{pop} = \begin{cases} C_L V_{DD}^2 \left[1 + 2A e^{-V_{DD}/nV_t}\right] & \text{Sub-threshold} \\ C_L V_{DD}^2 \left[1 + \dfrac{2A e^{-V_{DD}/nV_t}}{1 + (V_{DD} - V_T)^2 / 2V_t^2 (n-1)}\right] & \text{Just above threshold} \\ C_L V_{DD}^2 & \text{In strong inversion} \end{cases}$$

These expressions are plotted on the next slide.

Thanks to Naveen Verma for discussions on sub-threshold circuits.

Sub-threshold Circuit Design: Minimizing Energy per Operation in CMOS Logic

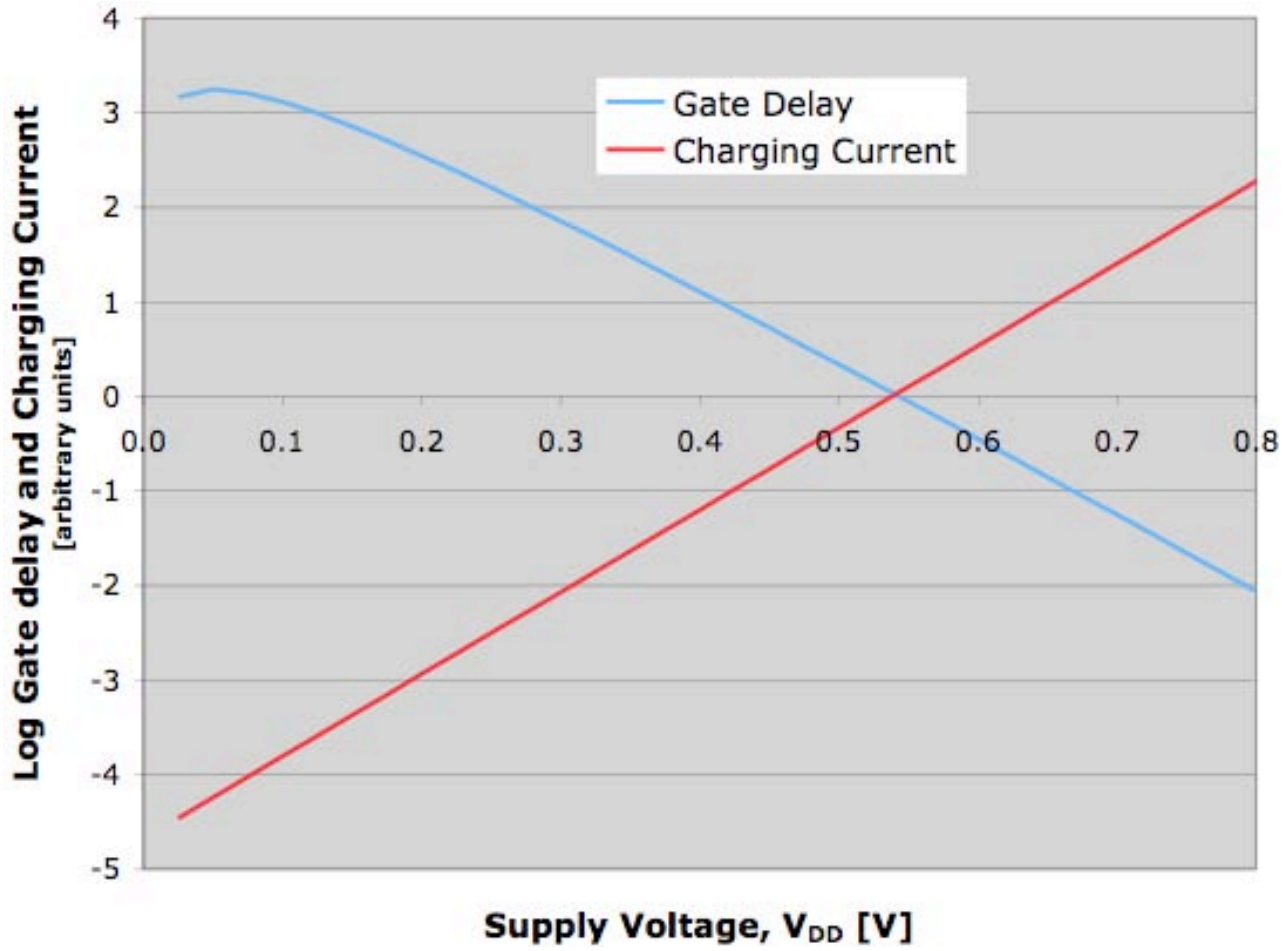
The energy per operation, E_{pop}, assuming $|V_T| = 0.4$ V, n = 2, and A = 50 and 100 is plotted below. Note the minimum for V_{DD} a bit below V_T:**



** The results are quite sensitive in detail to the values of n, A, and V_T.
Thanks to Naveen Verma for sub-threshold circuit discussions.

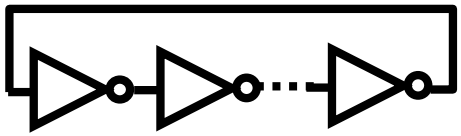
Sub-threshold Circuit Design: Minimizing Energy per Operation, cont.

Reducing V_{DD} reduces the charging/discharging currents rapidly and increases the cycle time significantly, so E_{min} operation is low speed.

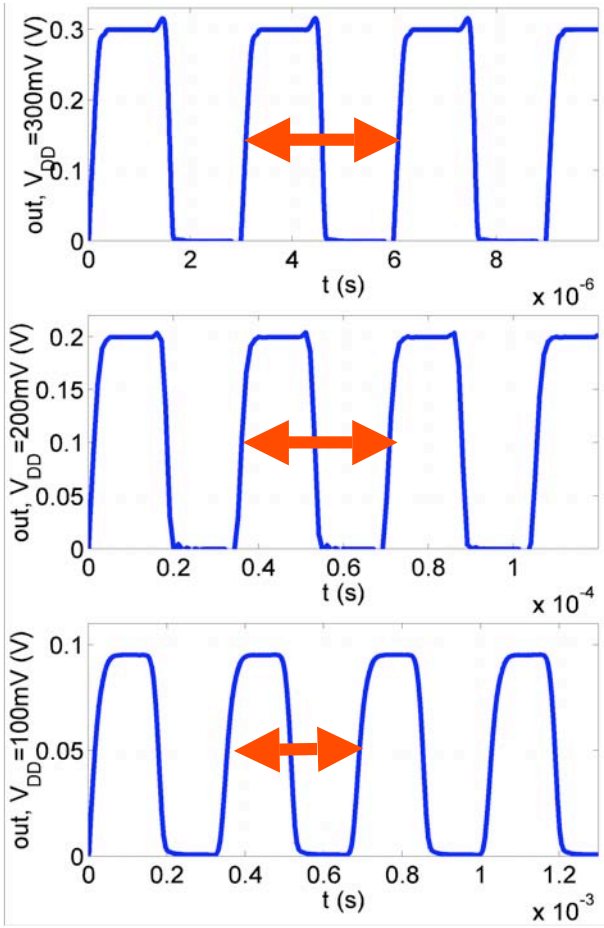


For many remote and monitoring sensor application this is just fine.

Sub-threshold Circuit Design: CMOS Inverters, cont.



11 stages



330kHz
300mV

29kHz
200mV

3kHz
100mV

- Simple ring oscillator shows functionality in deep sub V_T
- Delay increases exponentially in sub V_T

Work of Benton H. Calhoun at M.I.T. under Prof. Anantha Chandrakasan's supervision.

Sub-threshold Circuit Design: Linear circuits

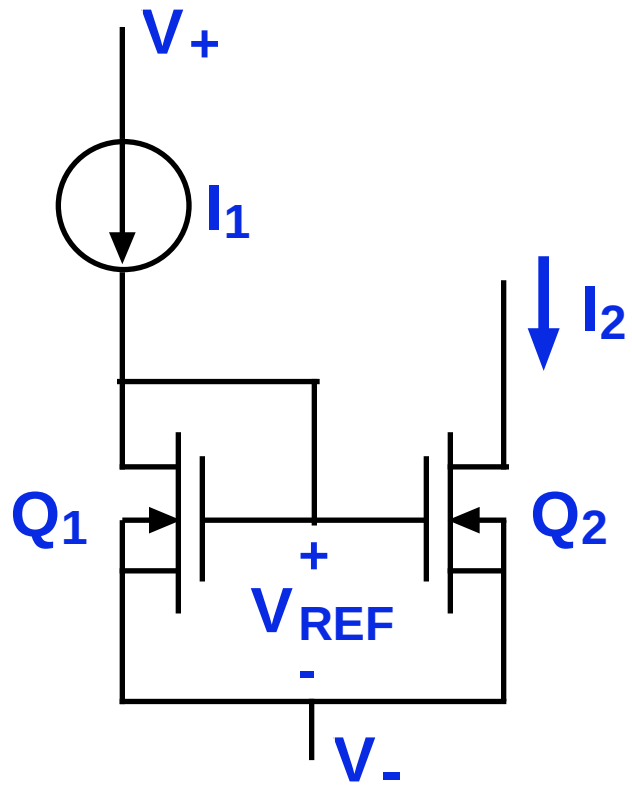
Conventional stages and designs can be operated in sub-threshold, just as was done with CMOS gates. They are slow, but if power is a concern and high speed isn't (i.e, under 10 MHz is OK), they are worth considering.

New types of MOS circuits are also possible: Translinear circuits.* Consider first, for example, the sub-threshold current mirror on the right:

$$V_{REF} - V_T = -n V_t \ln \frac{I_1}{W_1 I_{S,s-t}}$$

$$I_2 = W_2 I_{S,s-t} e^{-(V_{REF} - V_T)/nV_t} = \frac{W_2}{W_1} I_1$$

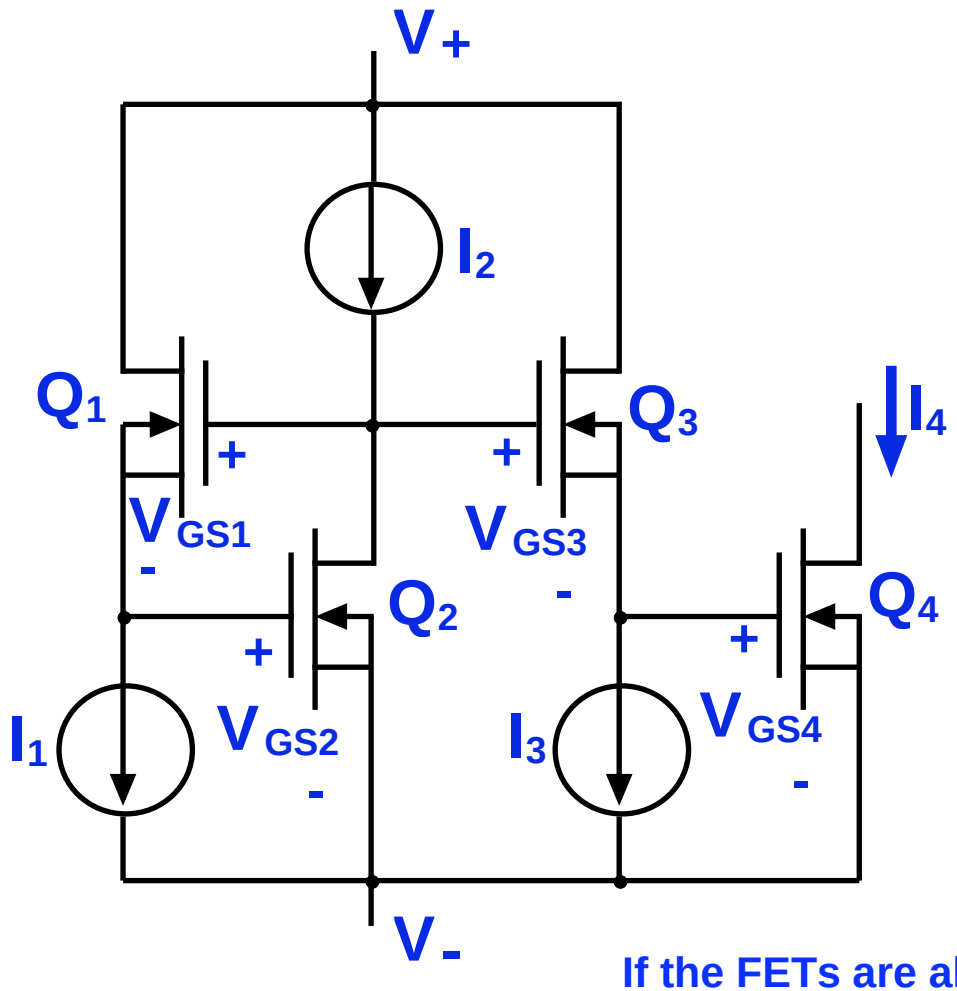
Note the exp to ln and ln to exp conversions.



* Translinear circuits were invented by Barrie Gilbert of Analog Devcies working with BJTs (IEEE JSSC, Vol SC-3, No. 4, Dec. 1968, pp. 353-373).

Sub-threshold Circuit Design: Translinear circuits, cont.

Now consider using this log function and its inversion to do multiplication. Consider the following circuit:



To begin note that:

$$v_{GS1} + v_{GS2} = v_{GS3} + v_{GS4}$$

and:

$$v_{GSi} - V_T = -nV_t \ln \frac{I_i}{W_i I_{S,s-t}}$$

Isolating v_{GS4}:

$$v_{GS4} = v_{GS1} + v_{GS2} - v_{GS3}$$

and substituting , we find:

$$I_4 = \frac{I_1 \cdot I_2}{I_3} \cdot \frac{W_3 \cdot W_4}{W_1 \cdot W_2}$$

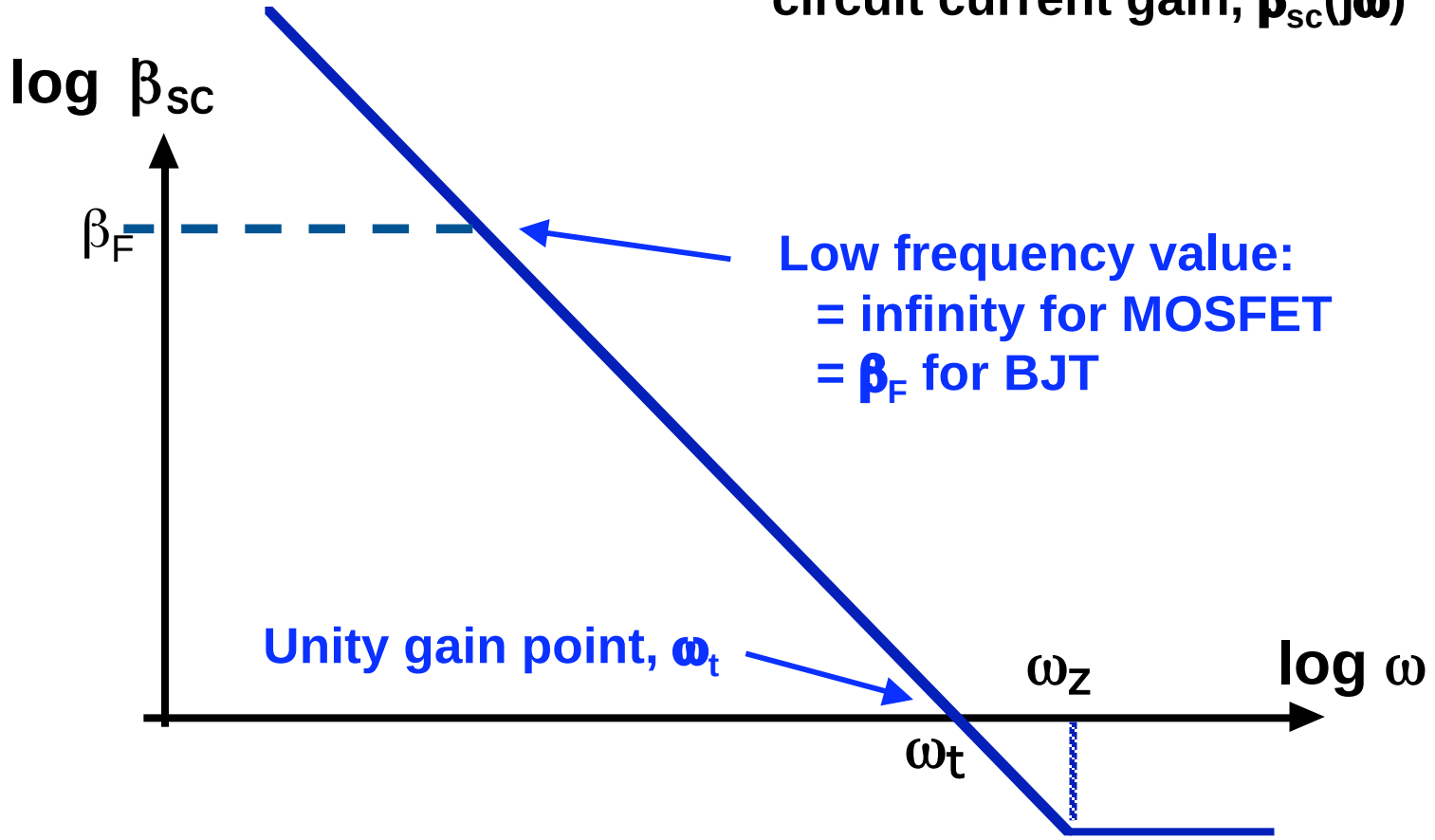
Circuits like this can be used to do analog multiplication.

If the FETs are all the same width:

$$I_4 = \frac{I_1 \cdot I_2}{I_3}$$

* After 6.376 notes via Naveen Verma.

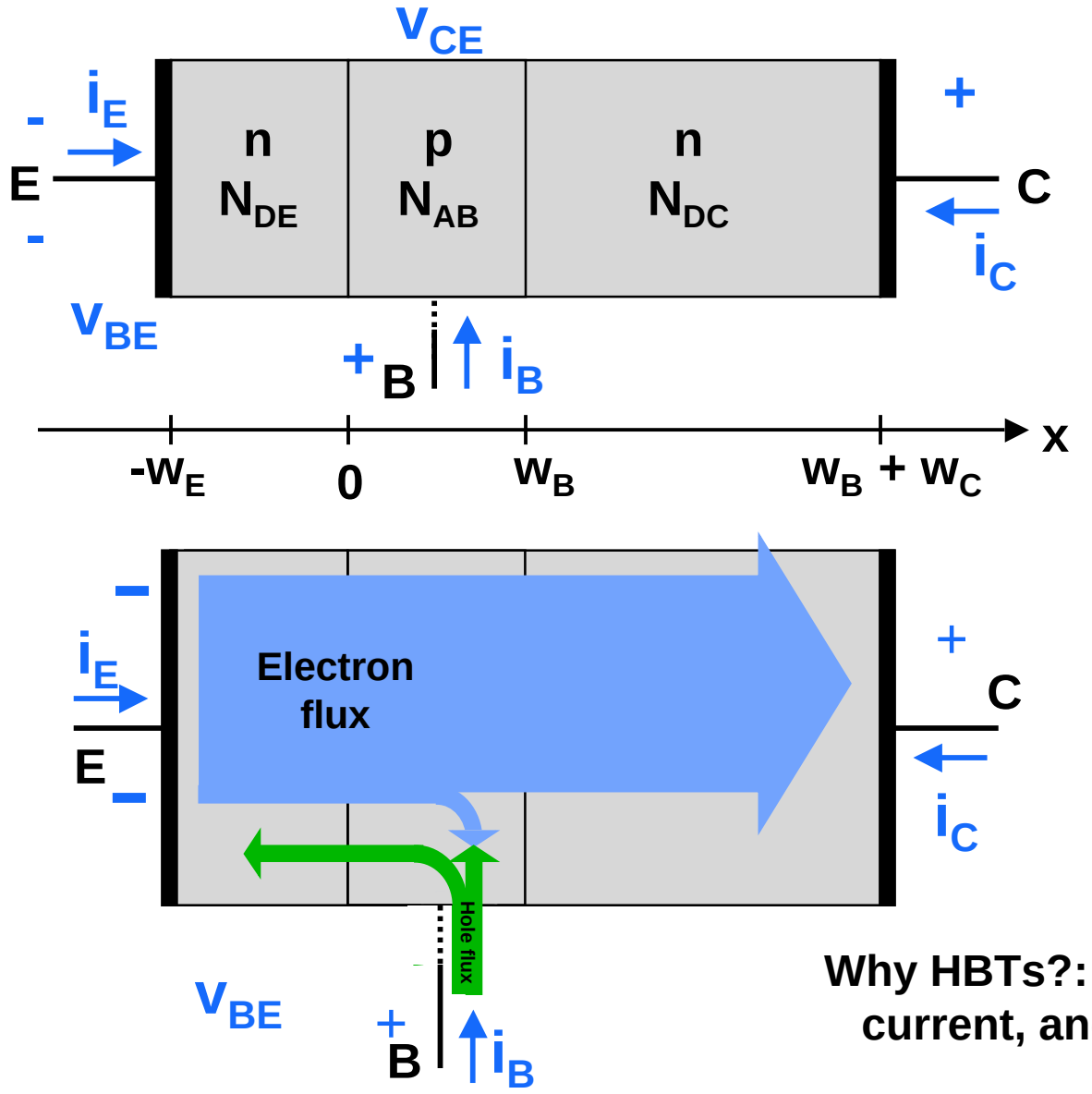
High frequency metric, f_T: unity gain point of the short-circuit current gain, $\beta_{sc}(j\omega)$



$$\omega_t \approx \begin{cases} g_m/C_{gs} = 3\mu_{Ch}(V_{GS}-V_T)/2L^2 = 3s_{Ch}/2L & \text{MOSFET, no vel. sat.} \\ g_m/C_{gs} = W\,s_{sat}C^*_{ox}/W\,LC^*_{ox} = s_{sat}/L & \text{MOSFET, w. vel. sat.} \\ g_m/(C_\pi + C_\mu) \Rightarrow \lim_{Ic\to\infty} \approx 2D_{\min,B}/w_B^2 & \text{BJT, large } I_C \end{cases} = \frac{1}{\tau_{tr}}$$

Bipolar Junction Transistors: basic operation and modeling…

… how the base-emitter voltage, v_{BE}, controls the collector current, i_C



Why HBTs?: high speed, current, and efficiency.

Heterojunction BipolarTransistors: higher mobility materials, graded base to create drift field, different E_g to tailor injection

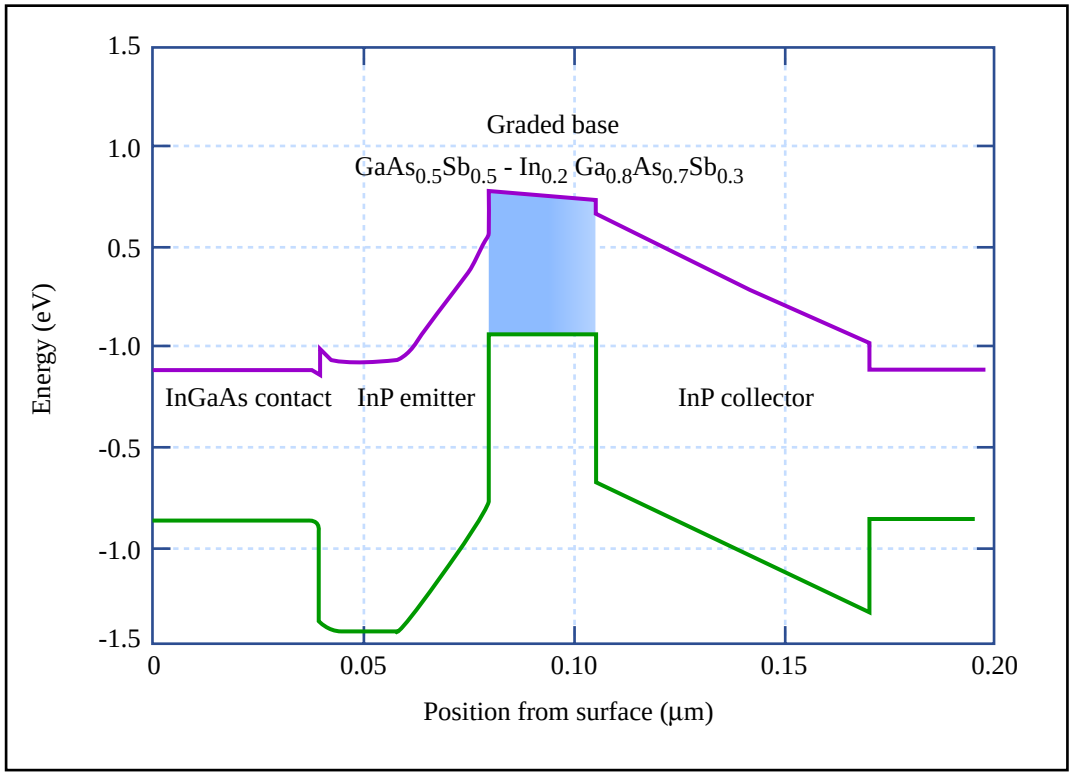


Figure by MIT OpenCourseWare.

Work of Prof. Milton Feng and students at University of Illinois

Source: Compound Semiconductor, March 2008

Heterojunction BipolarTransistors, cont: f_T = 685 GHz @ R.T.

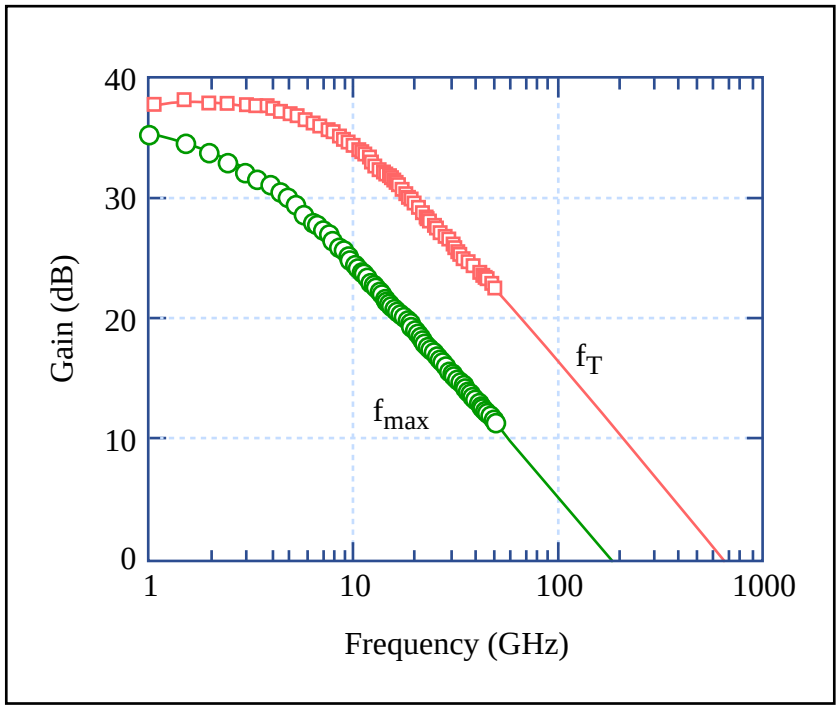


Figure by MIT OpenCourseWare.

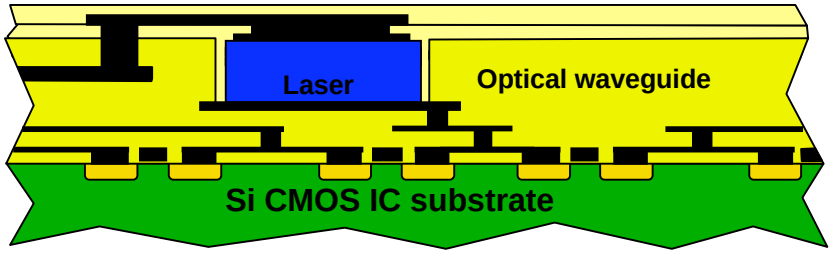
Notice that performance above 50-100 GHz is extrapolated using the theoretical frequency dependence to get f_T and f_{max} values. This is accepted practice because the instrumentation needed does not exist.

Source: Compound Semiconductor, March 2008

Mixing technologies and materials on a Si platform: other routes to keeping performance on the Si roadmap; optoelectronic integration

Coaxial coupling:

research at MIT



Evanescent vertical coupling:

work at UCSB and Intel

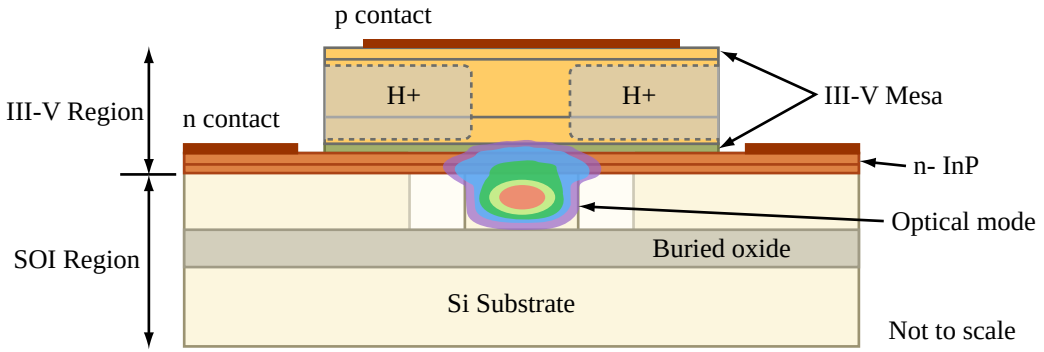
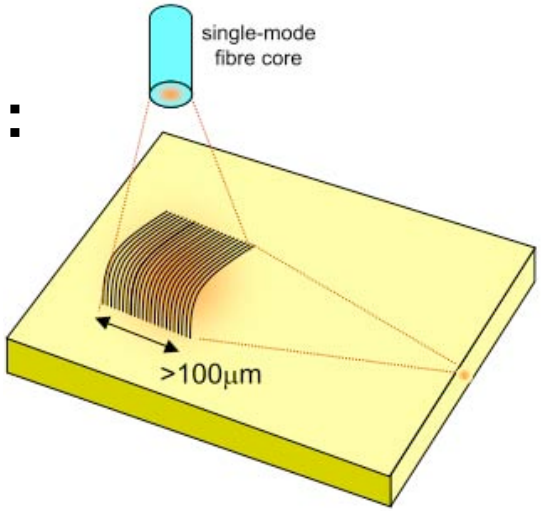


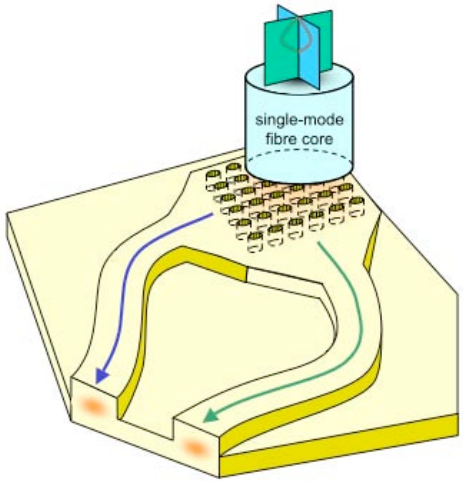
Figure by MIT OpenCourseWare.

Grating coupling:

specific to VCSELs

Source: Dirk Taillaert, INTEC, University of Gent



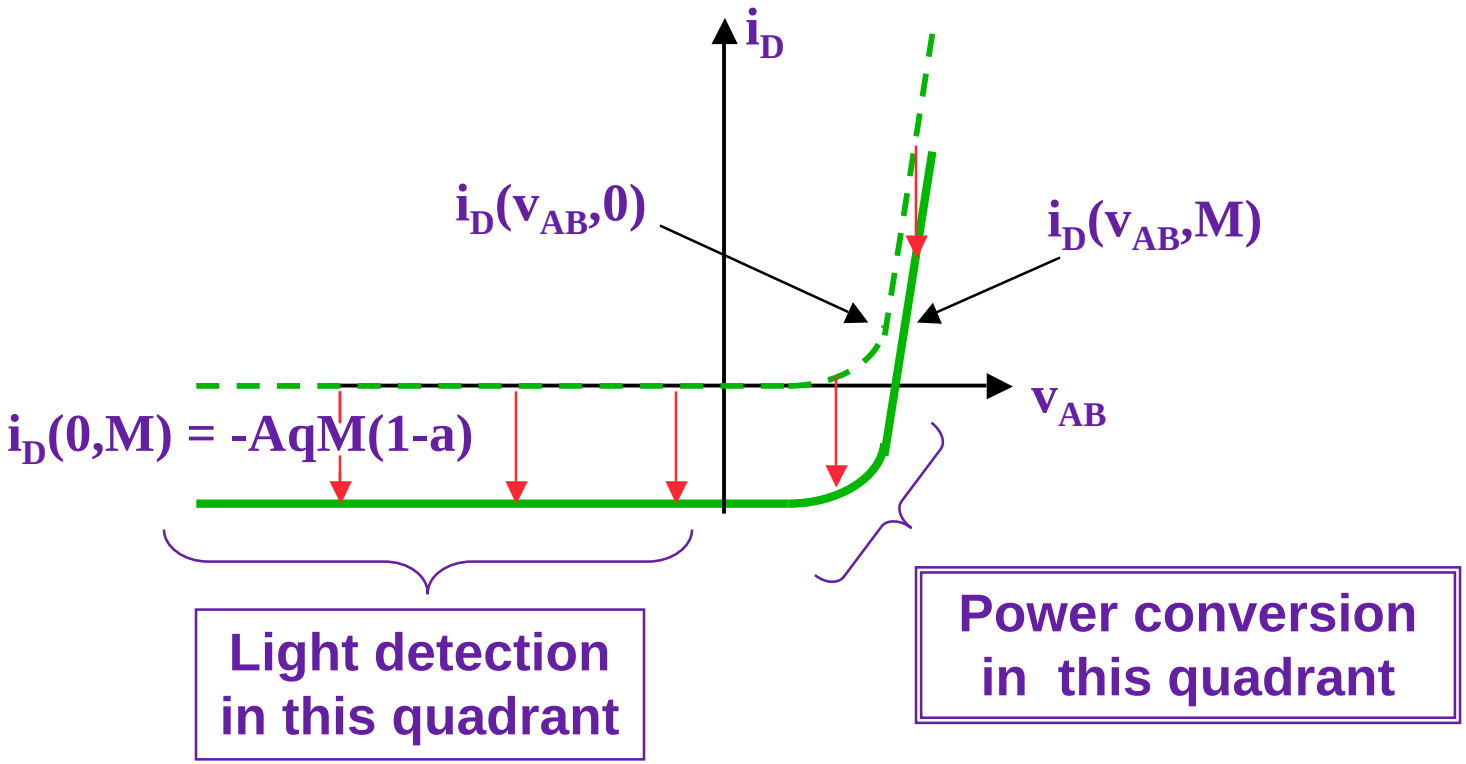


Solar Cells: Illumination shifts diode curve downward
Electrical power is produced in 4th quadrant

The total current:

$$i_D(v_{AB},M) = i_D(v_{AB},0) + i_D(0,M)$$
$$= I_S\left(e^{qv_{AB}/kT} - 1\right) - AqM(1-a)$$

Illumination shifts the ideal diode curve down vertically:

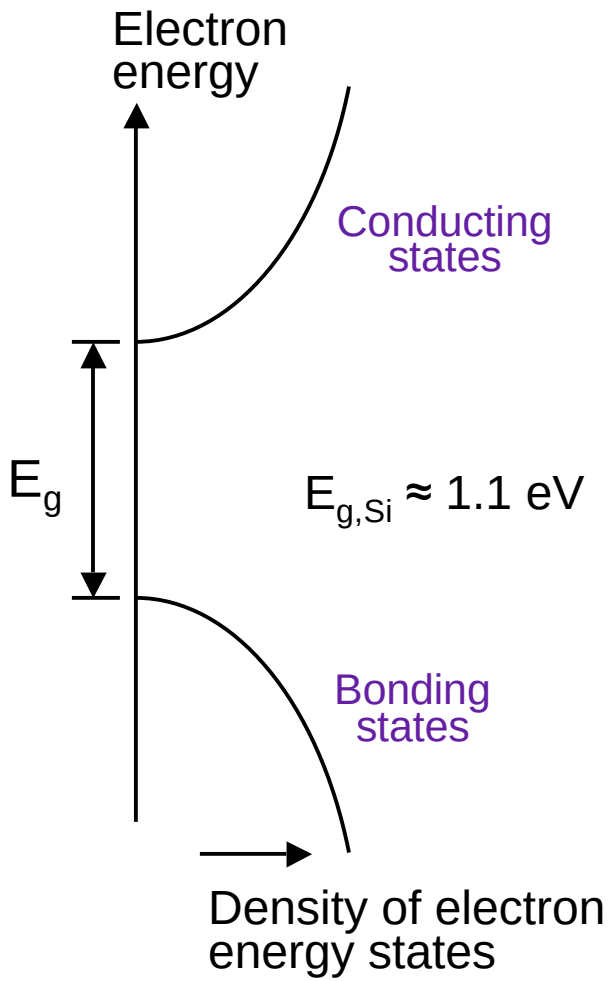


Solar Cells: A single band-gap diode misses much of the solar energy spectrum

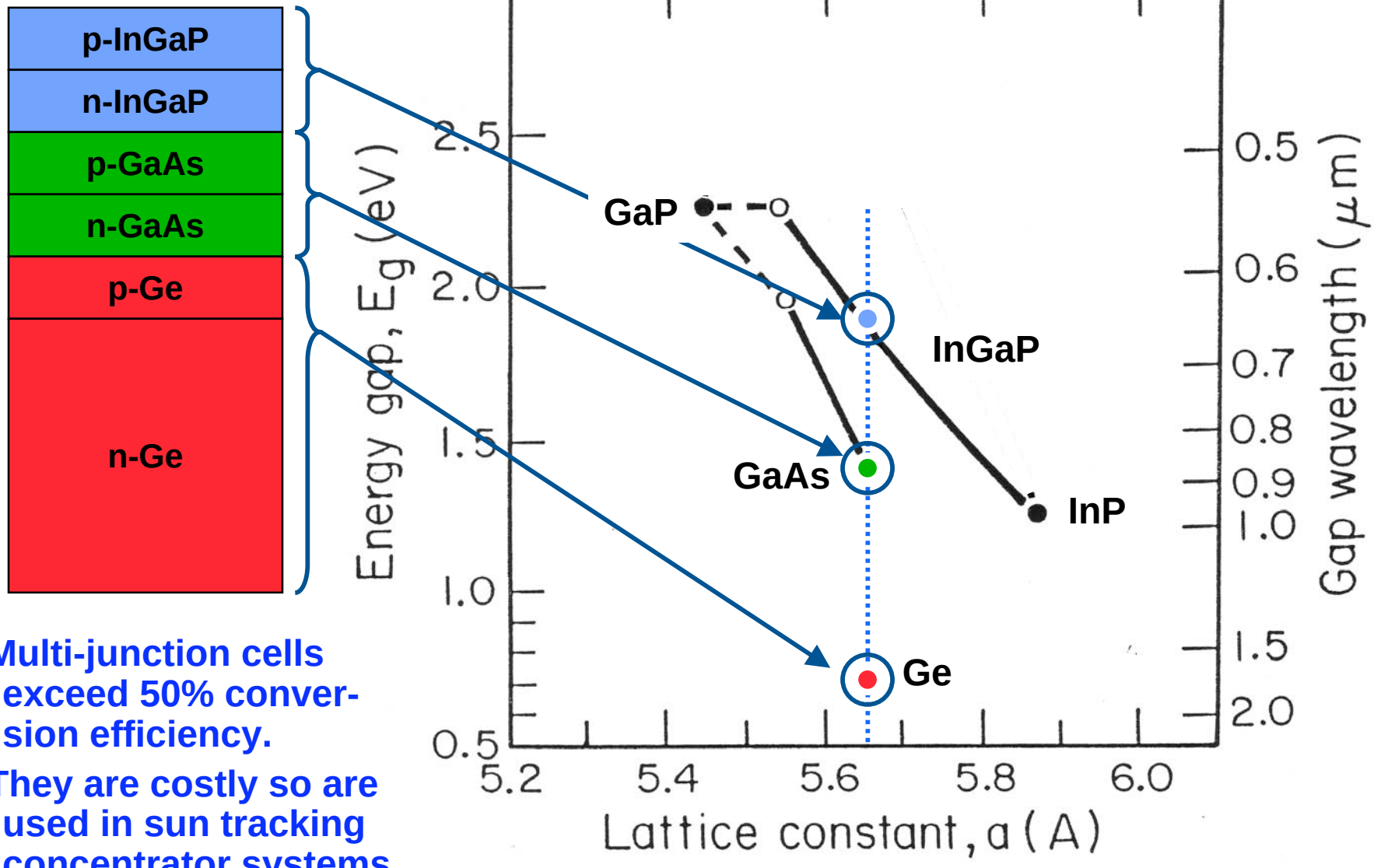
Photons with energy, $h\nu$, less than E_g are not absorbed, and that part of the spectrum is lost.

Photons with energy, $h\nu$, more than E_g are absorbed but all their energy above E_g is lost to the crystal lattice as the electrons and holes "relax" to the bottom of their the lowest energy states. This limits Si solar cell efficiency to ~ 20%.

The solution: Stack (layer) several solar cells with differing band-gaps so each optimally absorbs the optimum range of photons.



Solar Cells: Multi-junction solar cells InGaP/GaAs/Ge



Multi-junction cells exceed 50% conversion efficiency.

They are costly so are used in sun tracking concentrator systems.

Solar Cells: Multi-junction solar cells InGaP/GaAs/Ge, cont.

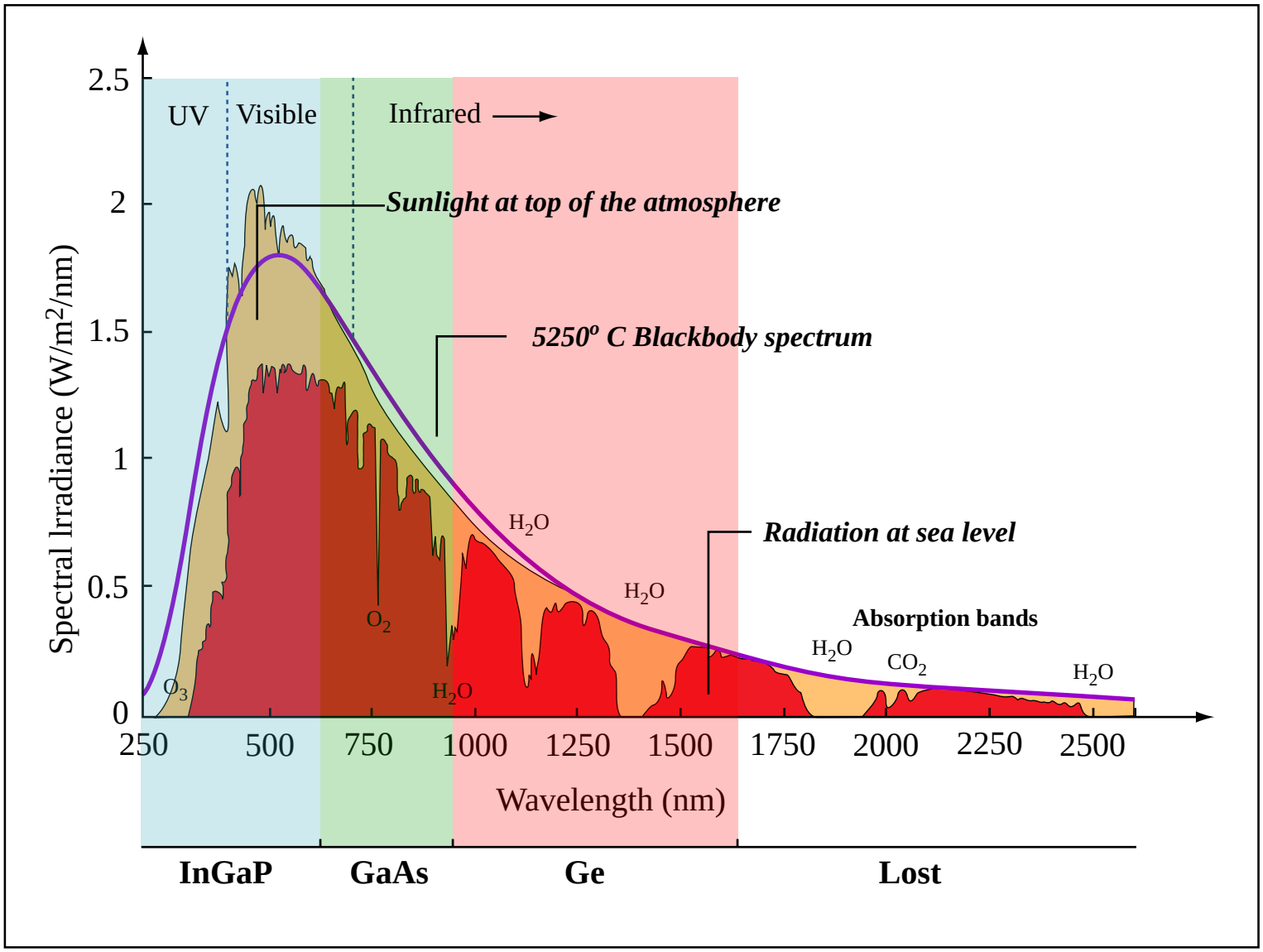
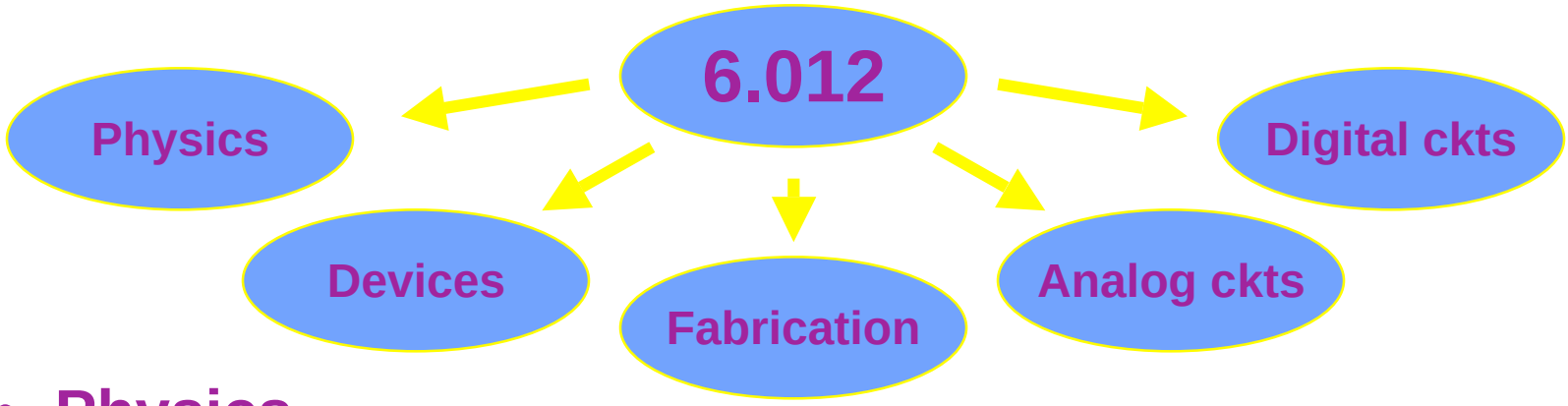


Figure by MIT OpenCourseWare.

Life after 6.012 - "I've taken the header, so…where can I head?"



- **Physics**

6.719:	Nano electronics (see also 6.701; similar but "U")	H	G(S)
6.728:	Applied quantum and statistical physics	H	G(F)
6.729:	Molecular electronics	H	G(S)
6.730:	Physics for solid-state applications	H	G(S)
6.732:	Physics of solids	H	G(F)
6.763:	Applied superconductivity	H	G(F*)

- **Devices**

6.720J:	Integrated microelectronic devices	H	G(F)
6.731:	Semiconductor optoelectronics	H	G(F*)
6.772:	Compound semiconductor devices	H	G(S*)
6.777J:	Design and fabrication of MEMS	H	G(S)
6.789:	Organic optoelectronics	H	G(S*)

Life after 6.012 - cont.

- **Processing**

6.152J:	Microelectronics processing technology		U(F,S)
6.774:	Physics of fabrication: front-end proc.	H	G(F*)
6.778J:	Materials and processes for MEMS	H	G(S)
6.780J:	Control of manufacturing processes	H	G(S*)
6.781J:	Sub-micron and nanometer technology	H	G(S)

- **Analog circuits**

6.301:	Solid-state circuits		G(F)
6.302:	Feedback systems		G(S)
6.331:	Advanced circuit techniques	H	G(F*)
6.334:	Power electronics	H	G(S)
6.376:	Low power analog VLSI	H	G(F)
6.775:	Design of analog MOS LSI	H	G(S)
6.776:	High speed communications circuits	H	G(S*)

- **Digital circuits**

6.374:	Analysis and design of digital ICs	H	G(F)
6.375:	Complex Digital Systems Design	H	G(S)

Lecture 25 - Beyond Si; Beyond 6.012 - Summary

- **The current state-of-the-art**
  - Very small and blazingly fast (and getting smaller and going faster every day)
  - L_{min} = 1.0 μm
    - → 0.75 μm
      - → 0.5 μm
        - → 0.35 μm
          - → 0.25 μm
            - → 0.18 μm
              - → 0.13 μm
                - → 90 nm
                - → 65 nm We're in this region now.
                - → 45 nm We're in this region now.
                - → 32 nm We're in this region now.
                - → 22nm
                - → 15 nm
                - → 11 nm
                - → 8 nm
                - → 5 nm

The world of semiconductor electronics encompasses far more than Si μP's and RAM, but it all benefits from the technology advances these major Si applications fund.

- **Life after 6.012**
  - Yes, there is life after 6.012.
    - → Physics
      - → Devices
        - → Processing
          - → Analog circuits
            - → Digital circuits

6.012 Microelectronic Devices and Circuits

Fall 2009