6.012 - Microelectronic Devices and Circuits

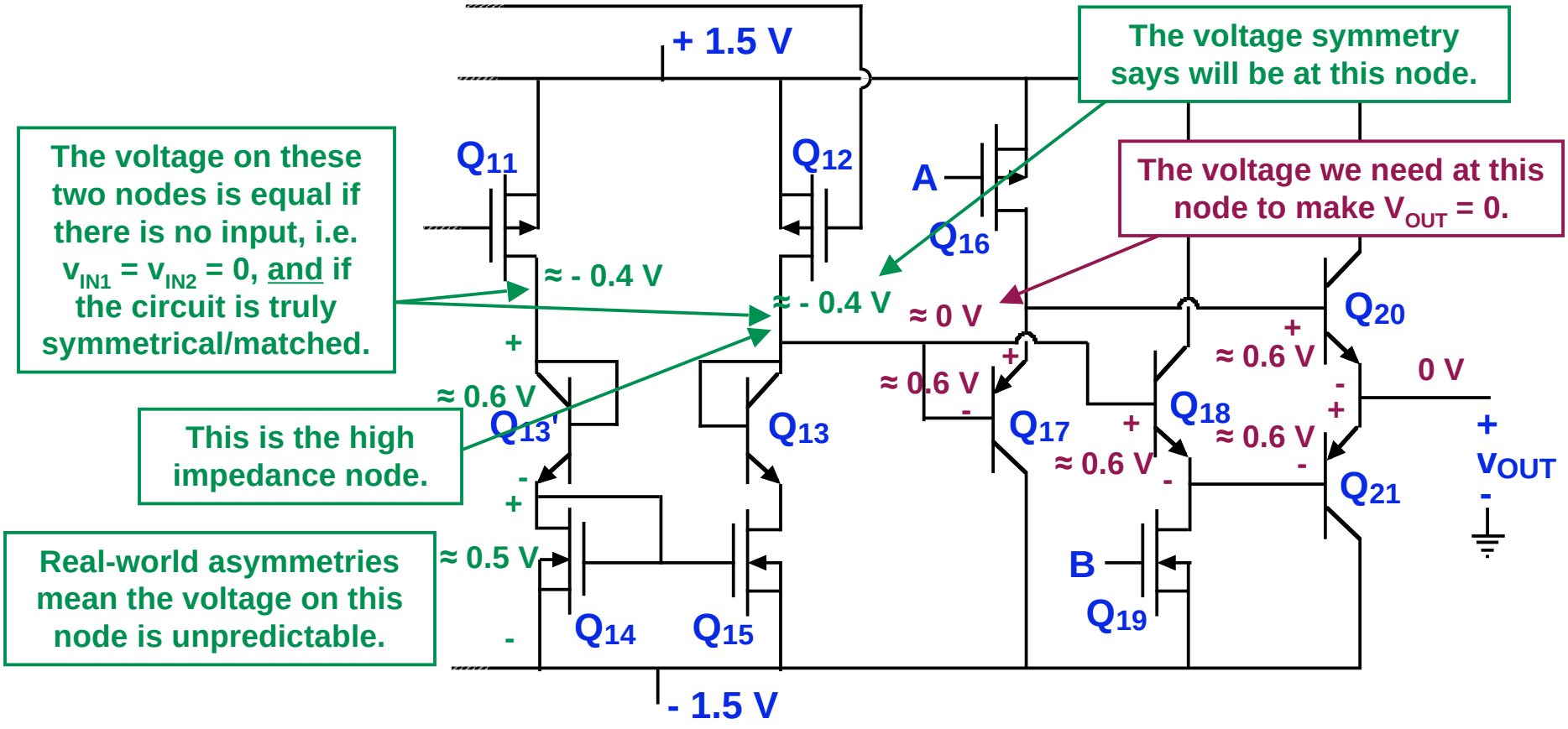
Lecture 22 - Diff-Amp Anal. III: Cascode, µA-741 - Outline

- **Announcements**
  - **DP:** Discussion of Q13, Q13' impact.
    Gain expressions.
- **Review - Output Stages**
  - DC Offset of an OpAmp
  - Push-pull/totem pole output stages
- **Specialty Stages, cont. - more useful transistor pairings**
  - The Marvelous Cascode
  - Darlington Connection
- **A Commercial Op-Amp Example - the µA-741**
  - The schematic and chip layout
  - Understanding the circuit
- **Bounding mid-band - starting high frequency issues**
  - Review of Mid-band concept
  - The Method of Open-Circuit Time Constants

DC off-set at the output of an Operational Amplifier:

DC off-set:

The node between Q_{12} and Q_{13} is a high impedance node whose quiescent voltage can only be determined by invoking symmetry.*



In any practical Op Amp, a very small differential input, v_{IN1}-v_{IN2}, is require to make the voltage on this node (and V_{OUT}) zero.

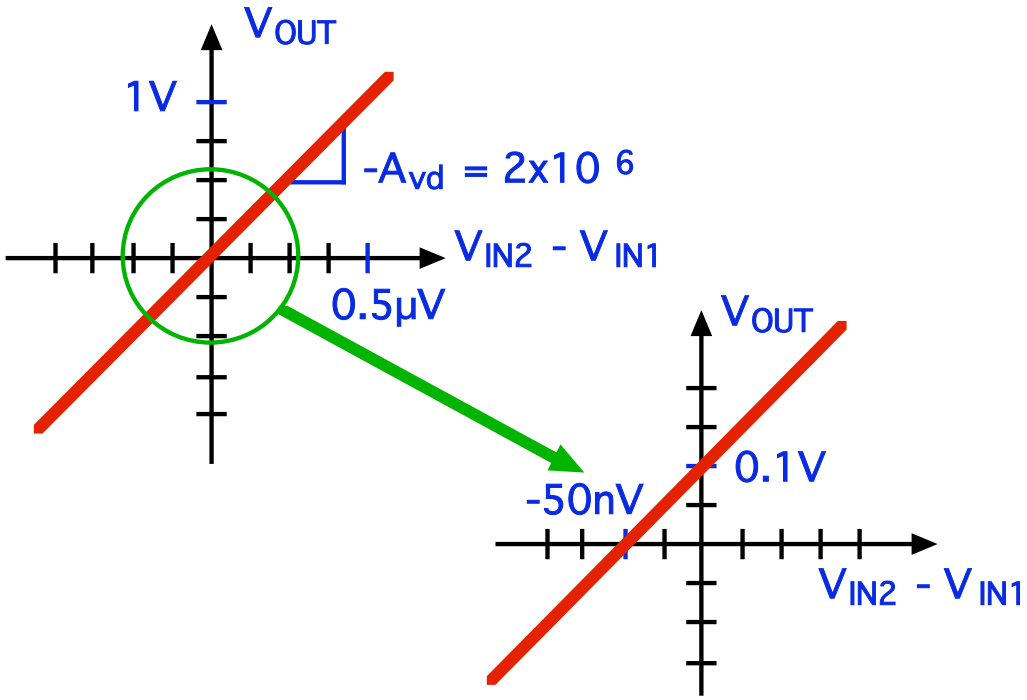
DC off-set at the output of an Op Amp, cont:

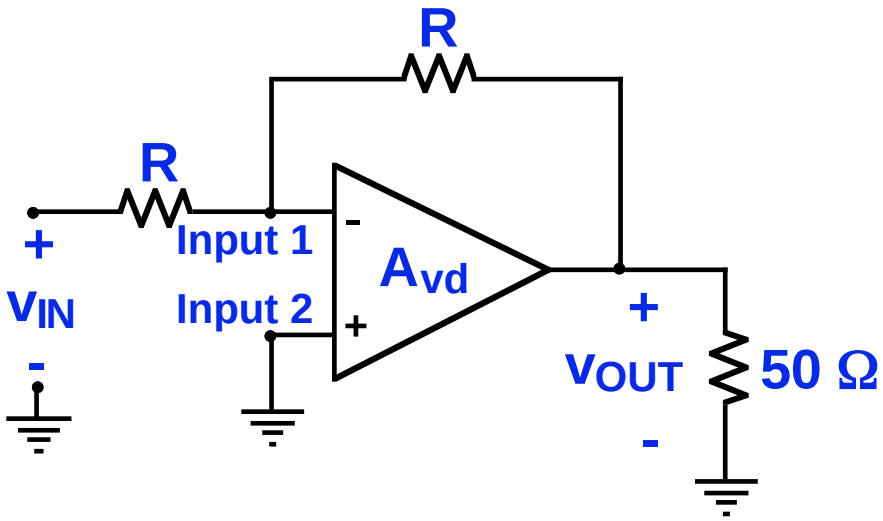
DC off-set:

The transfer characteristic, v_{OUT} vs $(v_{IN1} - v_{IN2})$, will not in general go through the origin, i.e.,

$$v_{OUT} = A_{vd}(v_{IN1} - v_{IN2}) + V_{OFFSET}$$

In the example in the figure A_{vd} is -2 x 10^6, and V_{OFFSET} is 0.1 V.





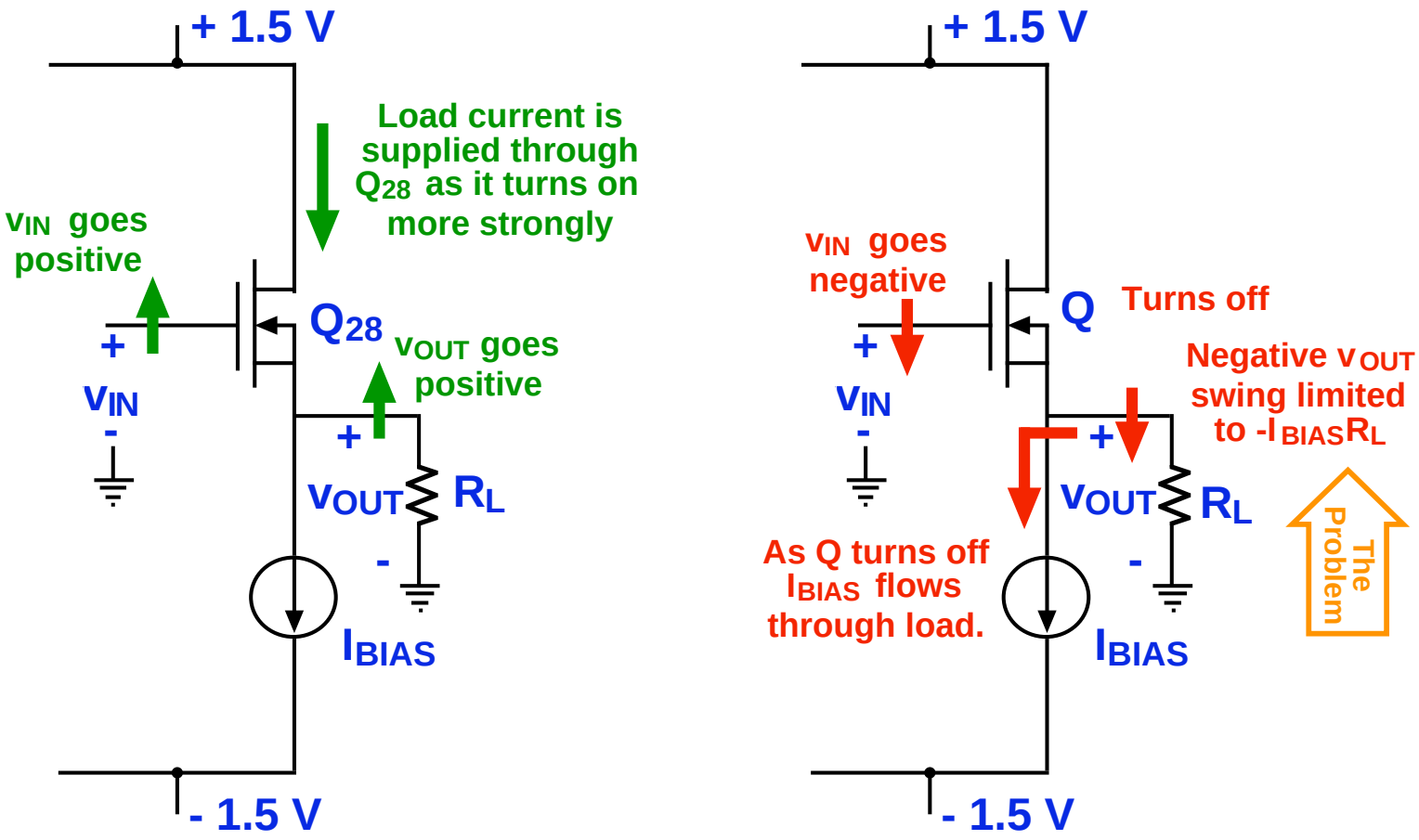
In a practice, an Op Amp will be used in a feed-back circuit like the example shown to the left, and the value of v_{OUT} with v_{IN} = 0 will be quite small. For this example (in which A_{vd} = -2 x 10^6, and V_{OFFSET} = 0.1 V) v_{OUT} is only 0.1 µV.

In the D.P. you are asked for this value for your design.

Specialty pairings: Push-pull or Totem Pole Output Pairs

A source follower output:

- Using a single source follower as the output stage must be biased with a relatively large drain current to achieve a large output voltage swing, which in turn dissipates a lot of quiescent power.

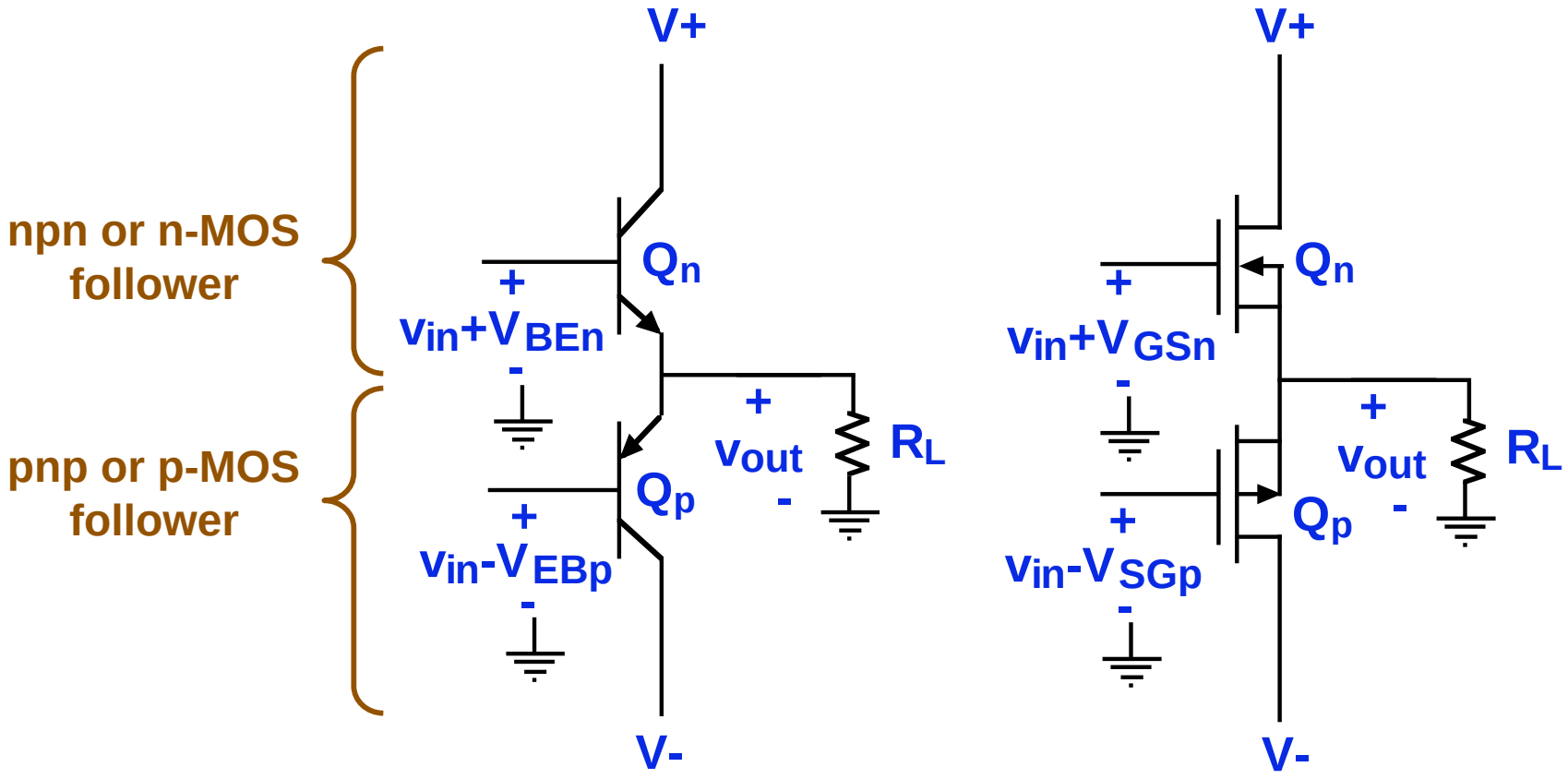


Specialty Pairings: The Push-pull or Totem Pole Output

A stacked pair of complementary emitter- or source-followers

Large input resistance
Small output resistance

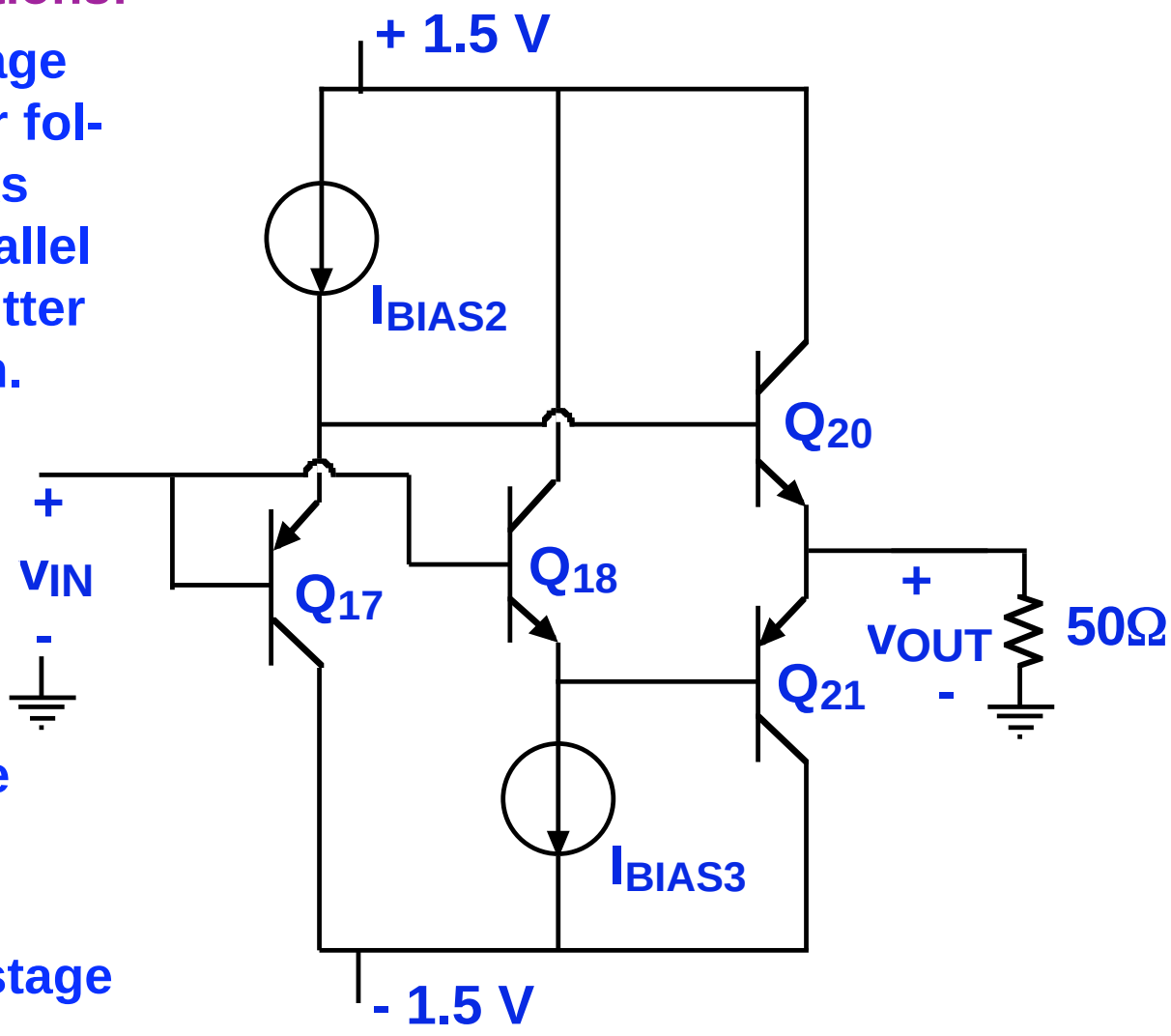
Voltage gain near one
Low quiescent power



Specialty pairings: Push-pull or Totem Pole in Design Prob.

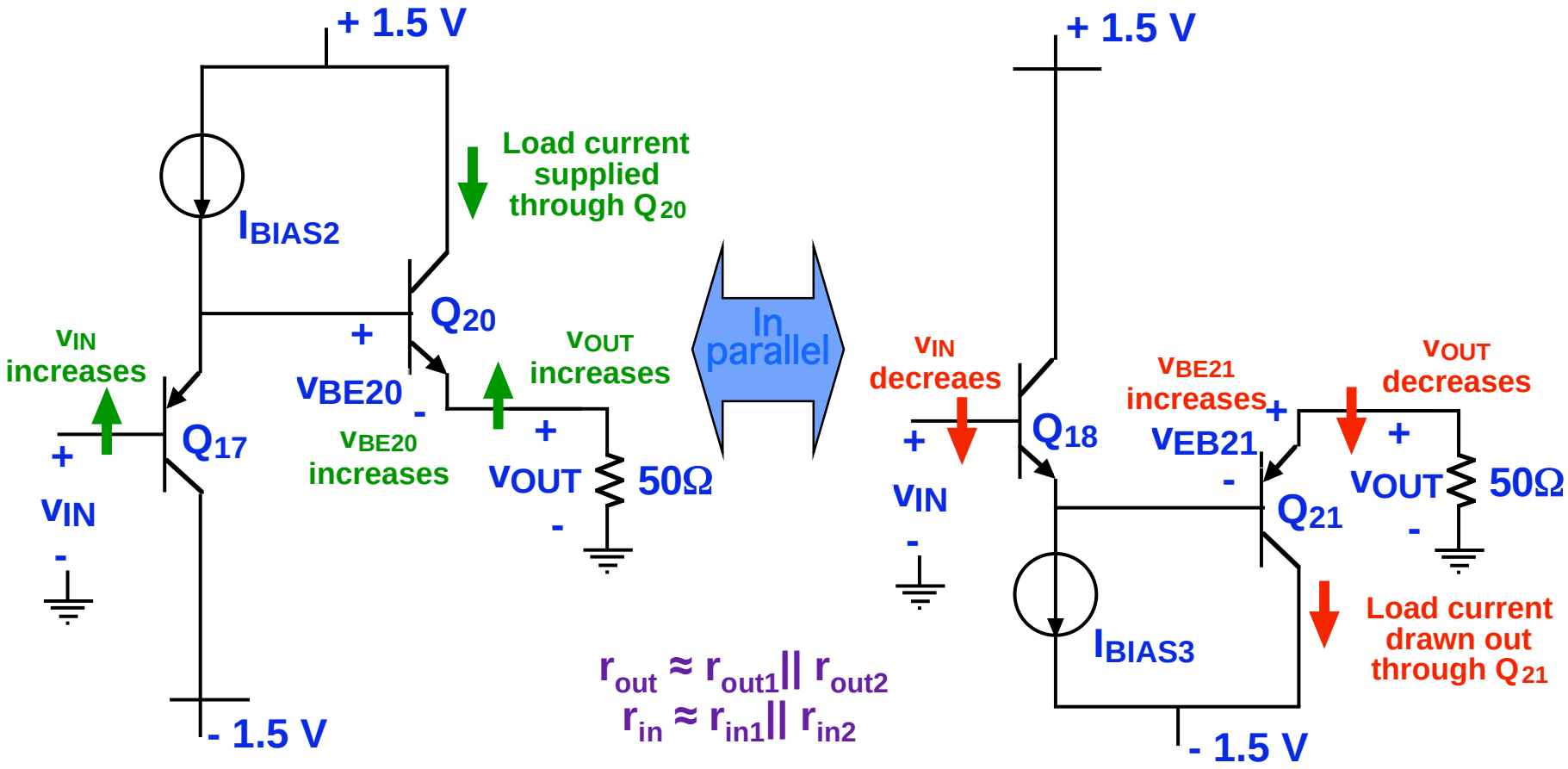
Comments/Observations:

- The D.P. output stage involves four emitter follower building blocks arranged as two parallel cascades of two emitter follower stages each.
- Q_{20} and Q_{21} with joined sources at the output node is called a push-pull, or totem pole pair.
- They determine the output resistance of the amplifier.
- Ideally the output stage voltage gain is ≈ 1.



Specialty pairings: Push-pull or Totem Pole in D.P., cont.

Operation: The npn follower supplies current when the input goes positive to push the output up, while the pnp follower sinks current when the input goes negative to pull the output down.

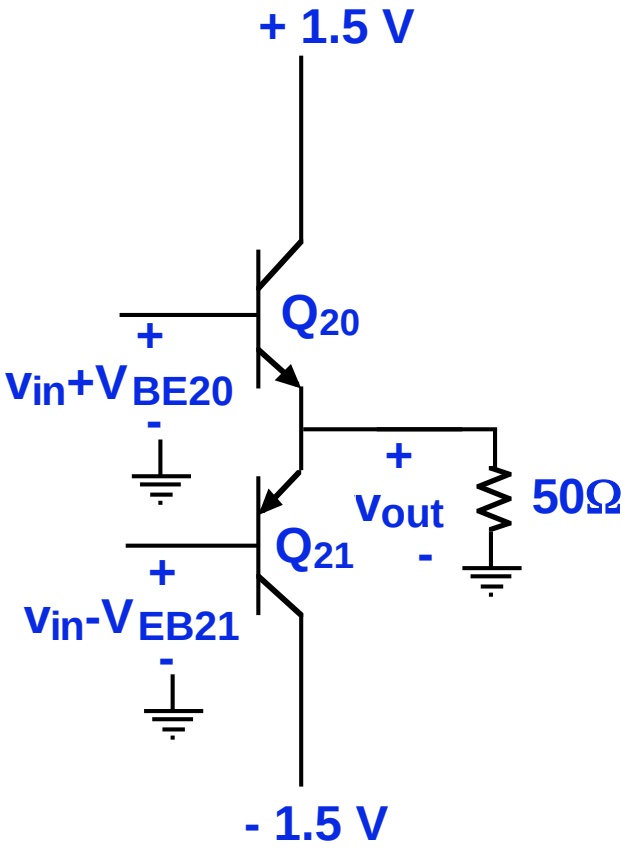


- The input resistance, r_{out}, is highest about zero output, and there it is the output resistance of the two follower stages in parallel.
- r_{in} is lowest at this point, too, and is a parallel combination, also.

Specialty pairings: Push-pull or Totem Pole, cont.

Voltage gain:

- The design problem uses a bipolar totem pole. The gain and linearity of this stage depend on the bias level of the totem pole. The gain is higher for with higher bias, but the power dissipation is also.



To calculate the large signal transfer characteristic of the bipolar totem pole we begin with v_{OUT}:

$$v_{OUT} = R_L\left(-i_{E20} - i_{E21}\right)$$

The emitter currents depend on $(v_{IN} - v_{OUT})$:

$$i_{E20} = -I_{E20}e^{(v_{IN}-v_{OUT})/V_t}, \quad i_{E21} = I_{E21}e^{-(v_{IN}-v_{OUT})/V_t}$$

Putting this all together, and using $I_{E21} = -I_{E20}$, we have:

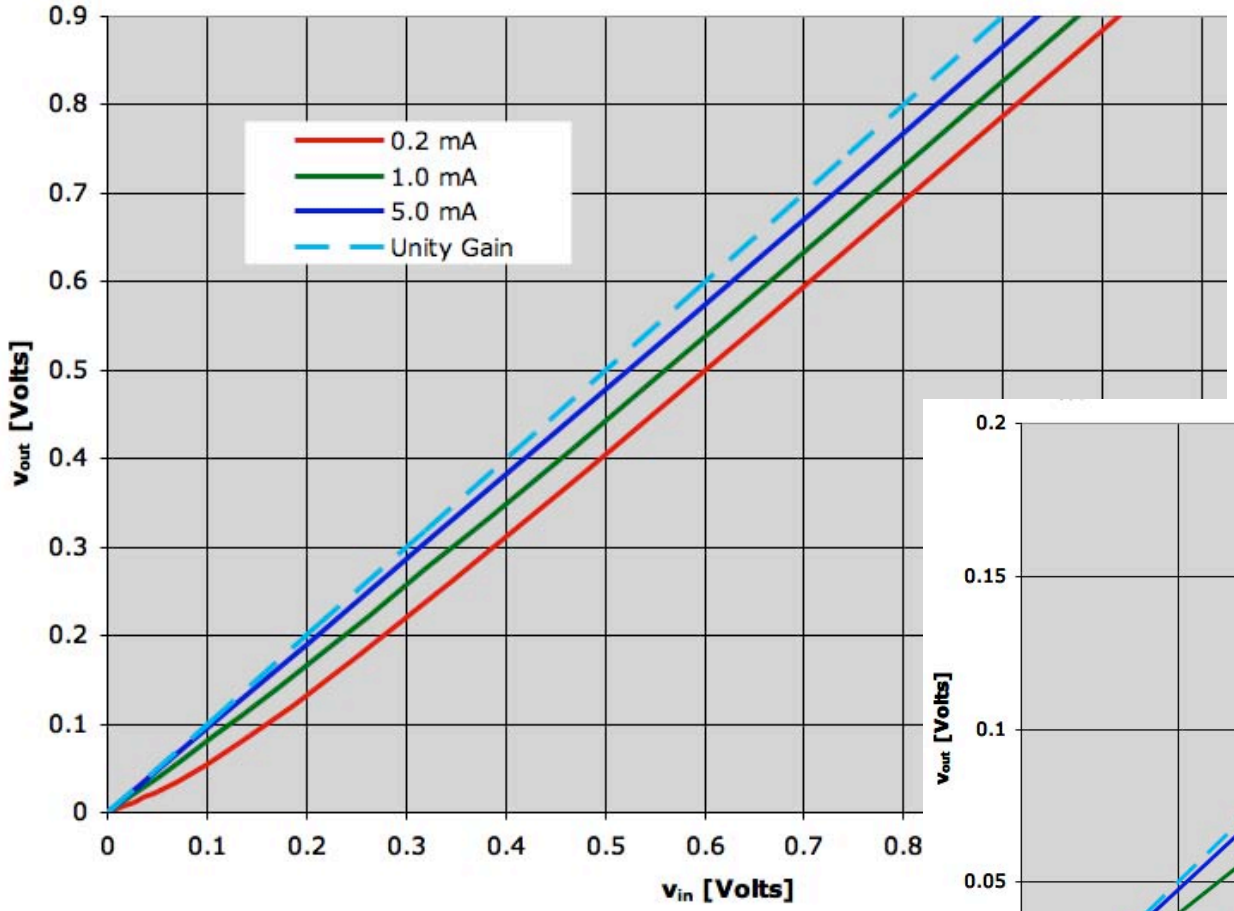
$$v_{out} = R_L I_{E20}\left(e^{(v_{in}-v_{out})/V_t} - e^{-(v_{in}-v_{out})/V_t}\right)$$

$$= 2R_L I_{E20}\sinh\left(v_{in} - v_{out}\right)/V_t$$

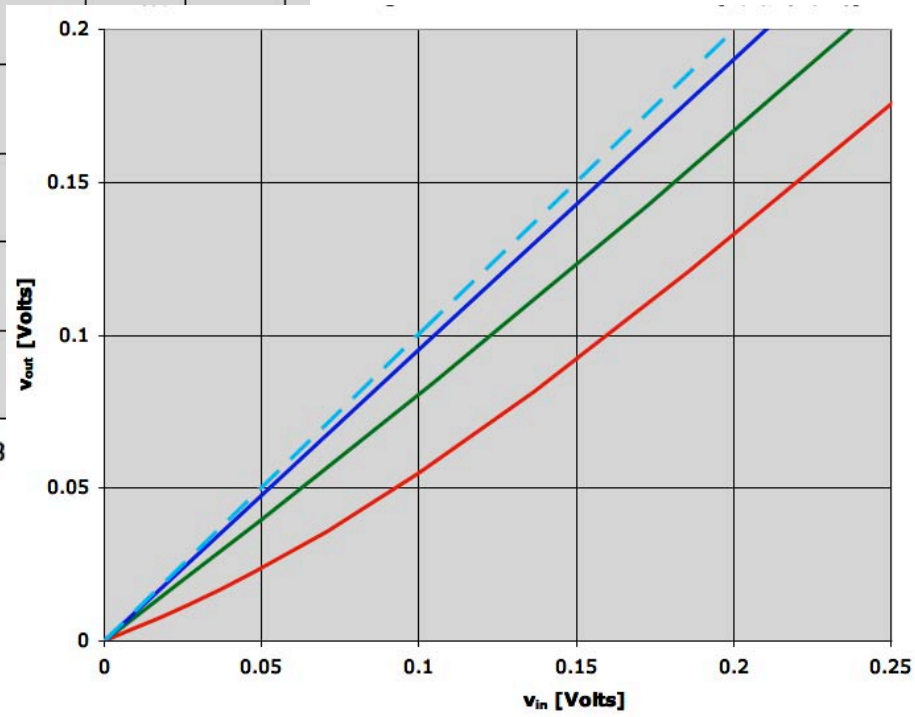
We can do a spread-sheet solution by picking a set of values for $(v_{IN} - v_{OUT})$, using the last equation to calculate the v_{OUT}, using this v_{OUT} to calculate v_{IN}, and finally plotting v_{OUT} vs v_{IN}. The results are seen on the next slide.

Voltage gain, cont.:

- With a 50 Ω load and for several different bias levels we find:

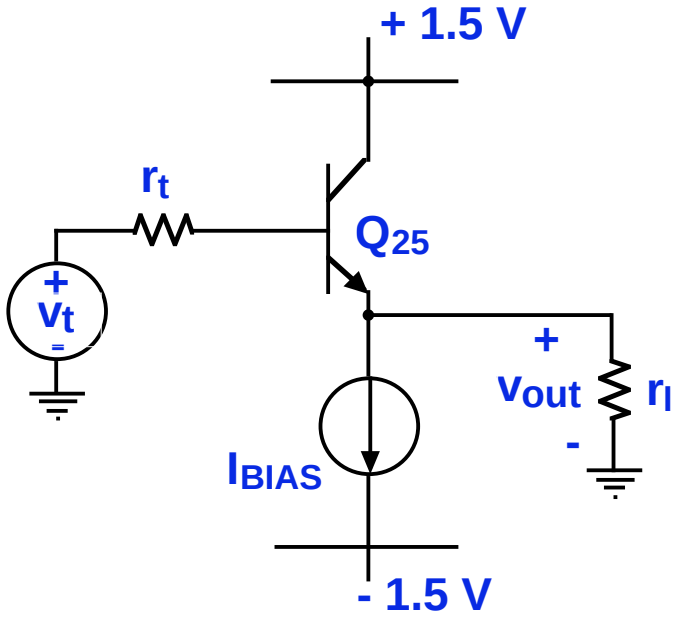


The gain and linearity are improved by increasing the bias current, but the cost is increased power dissipation.

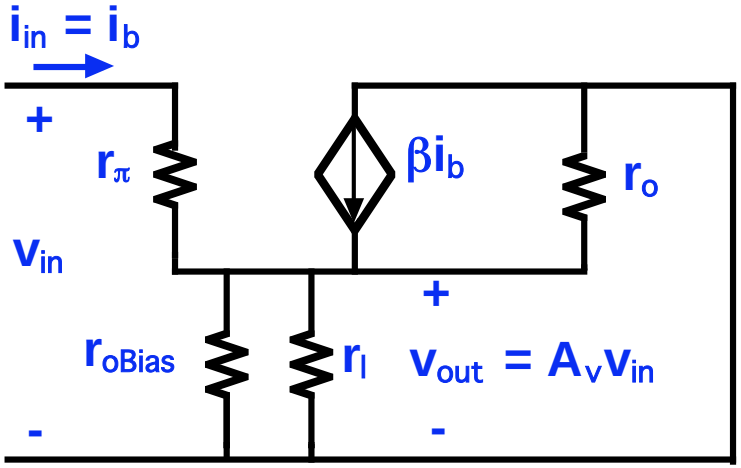


The A_v is lowest and r_{out} is highest at the bias point (i.e., $V_{IN} = V_{OUT} = 0$). r_{in} to the stage is also lowest there.

Specialty pairings: Push-pull or Totem Pole in D.P., cont.



Reviewing the voltage gain of an emitter follower:



$$v_{out} = (\beta+1) i_b (r_l \,||\, r_o \,||\, r_{Bias})$$

$$v_{in} = i_b r_\pi + (\beta+1) i_b (r_l \,||\, r_o \,||\, r_{Bias})$$

$$A_v = \frac{v_{out}}{v_{in}} = \frac{(\beta+1)(r_l \,||\, r_o \,||\, r_{Bias})}{r_\pi + (\beta+1)(r_l \,||\, r_o \,||\, r_{Bias})}$$

$$\approx \frac{(\beta+1) r_l}{r_\pi + (\beta+1) r_l}$$

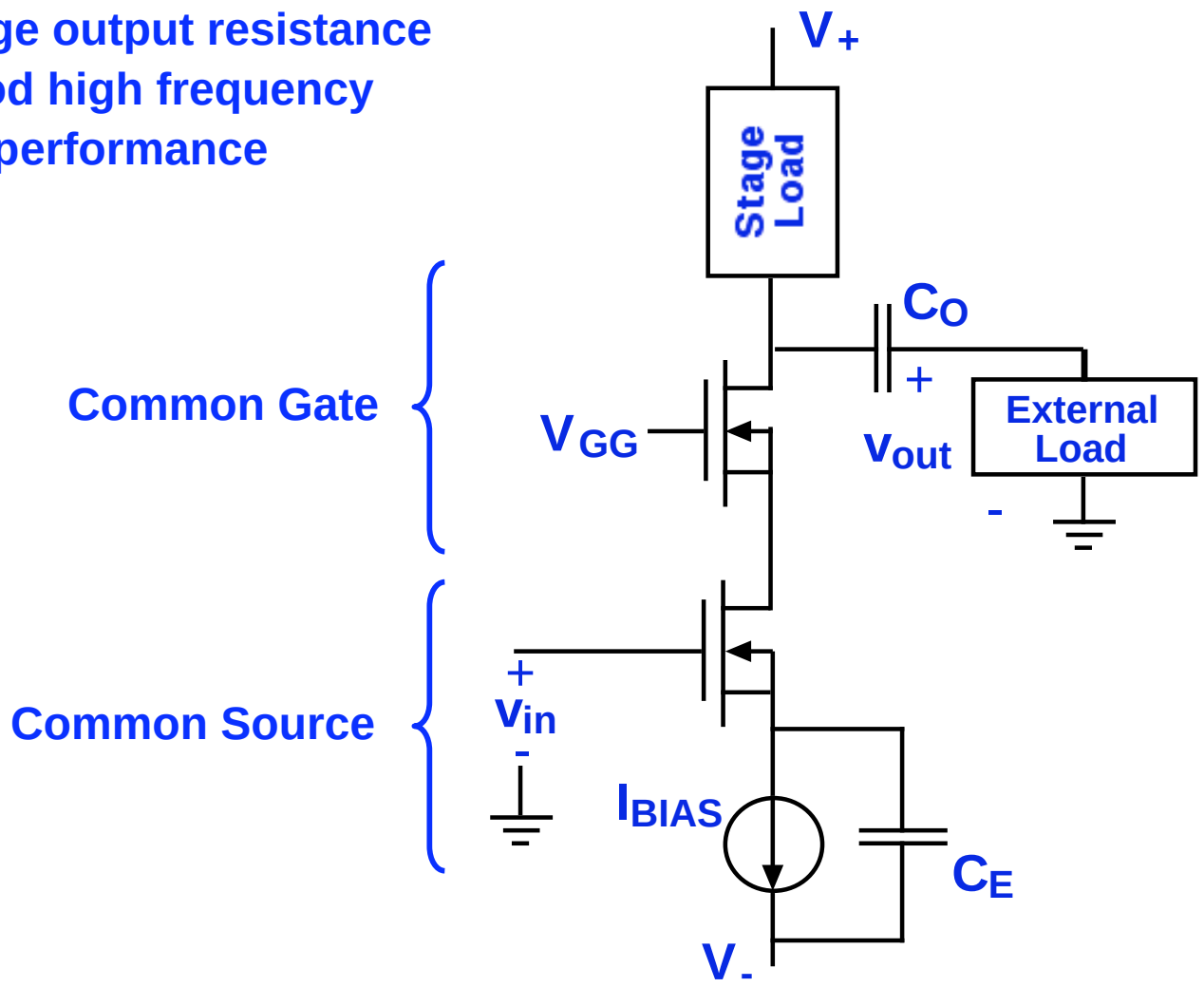
Note:

- The voltage gains of the third-stage emitter followers (Q_{25} and Q_{26}) will likely be very close to one, but that of the stage-four followers might be noticeably less than one.

Specialty Pairings: The Cascode

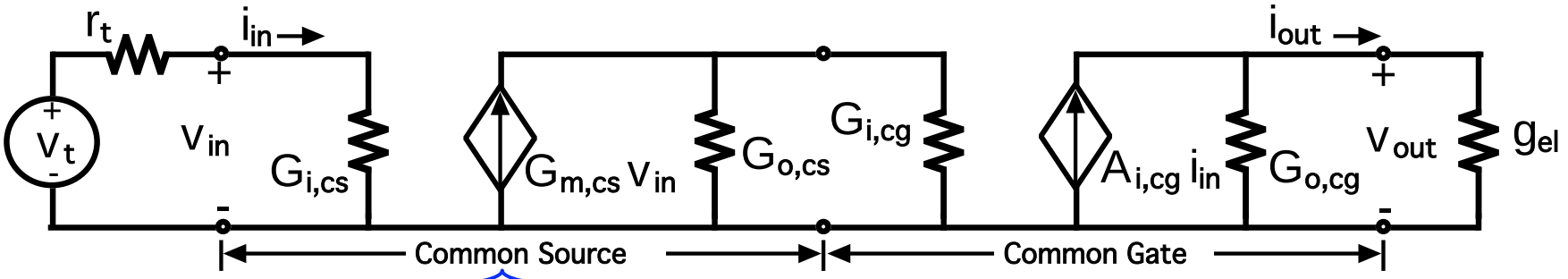
Common-source stage followed by a common gate stage

Large output resistance
Good high frequency performance



Specialty Pairings: The Cascode, cont.

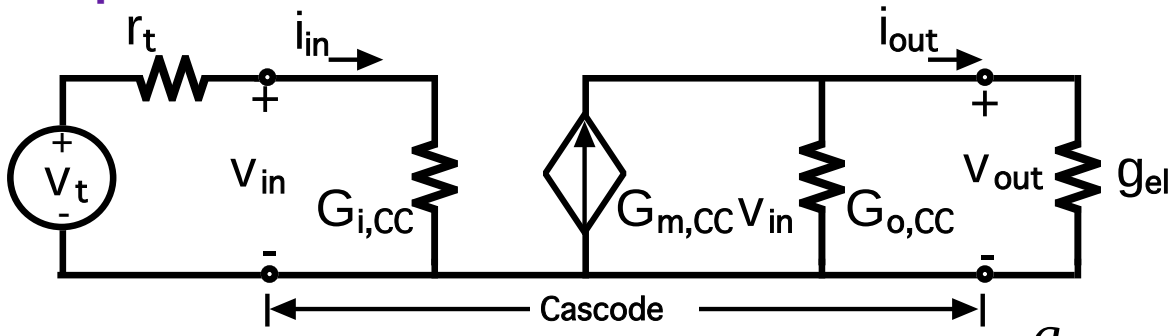
Two-Port Analysis



$$G_{i,cs} = 0,\ G_{m,cs} = -g_{m,Q_{cs}},\ G_{o,cs} = g_{o,Q_{cs}}$$

$$G_{i,cg} = g_{m,Q_{cg}},\ A_{i,cg} = 1,\ G_{o,cg} \approx g_{o,Q_{cs}} \frac{g_{o,Q_{cg}}}{g_{m,Q_{cg}}}$$

Cascode two-port:

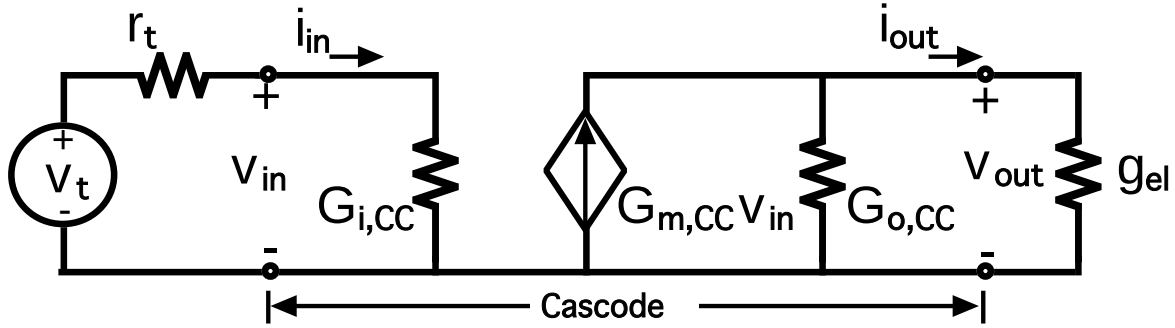


$$G_{i,CC} = 0,\ G_{m,CC} \approx -g_{m,Q_{cs}},\ G_{o,CC} \approx g_{o,Q_{cs}} \frac{g_{o,Q_{cg}}}{g_{m,Q_{cg}}}$$

Same G_i and G_m of CS stage, with the very much larger G_o of CG.

Specialty Pairings: The Cascode, cont.

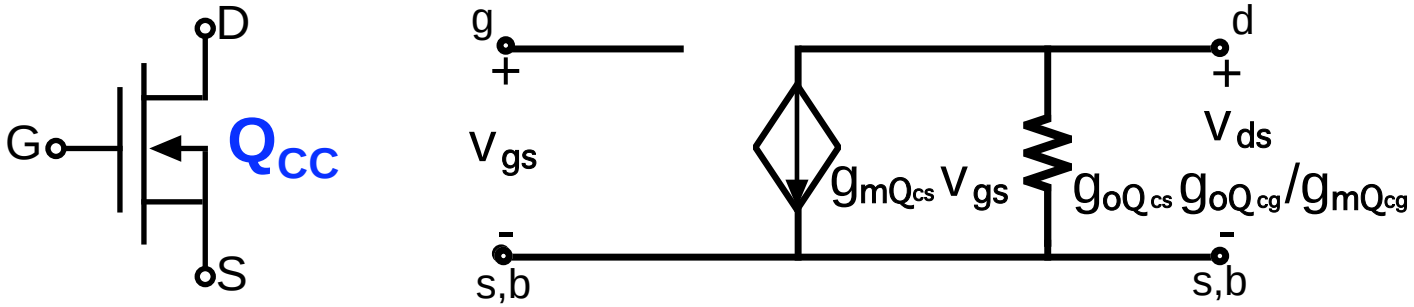
Cascode two-port:



$$G_{i,CC} = 0,\ G_{m,CC} \approx -g_{m,Q_{cs}},\ G_{o,CC} \approx g_{o,Q_{cs}} \frac{g_{o,Q_{cg}}}{g_{m,Q_{cg}}}$$

The equivalent Cascode transistor:

The cascode two-port is that of a single MOSFET with the g_m of the first transistor, and the output conductance of common gate.

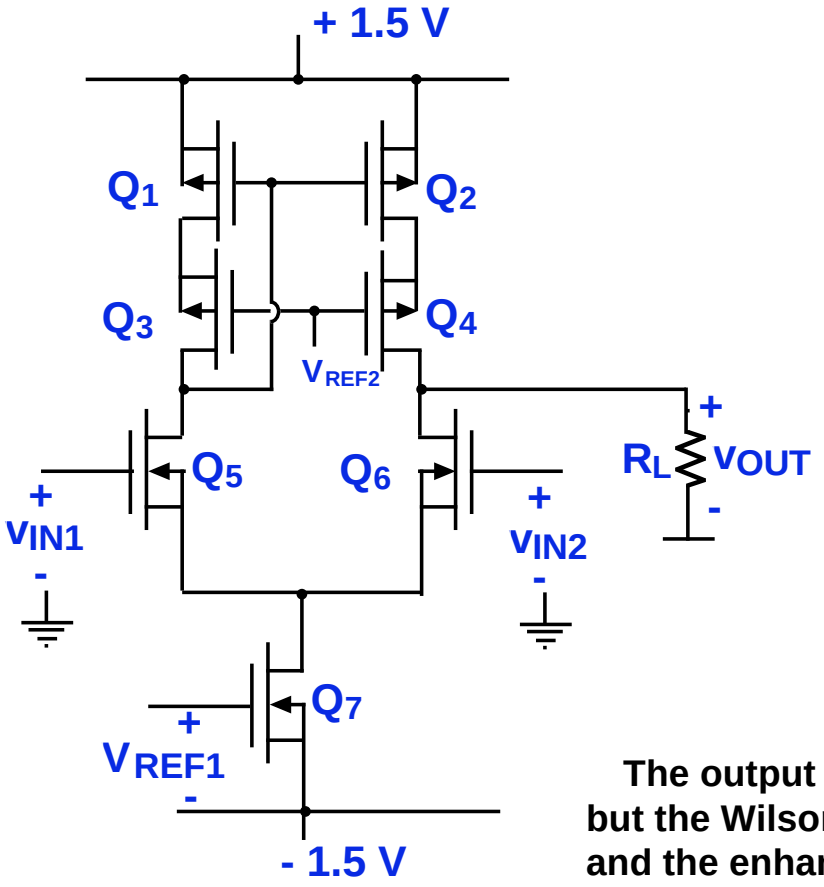


Specialty Pairings: The Cascode, cont.

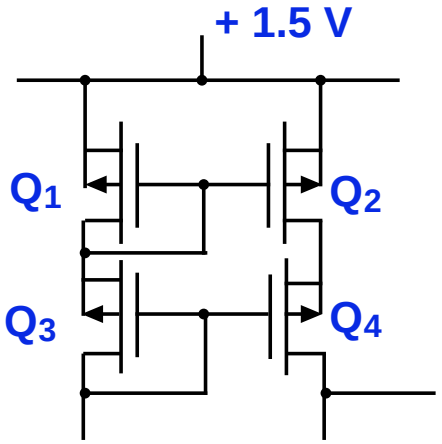
Cascode current mirrors: alternative connections

Large differential output resistance

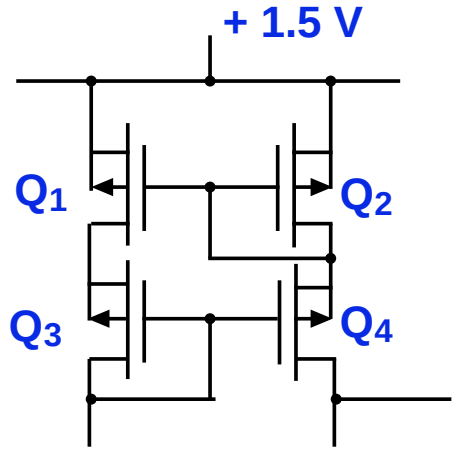
Enhanced swing cascode



Classic cascode

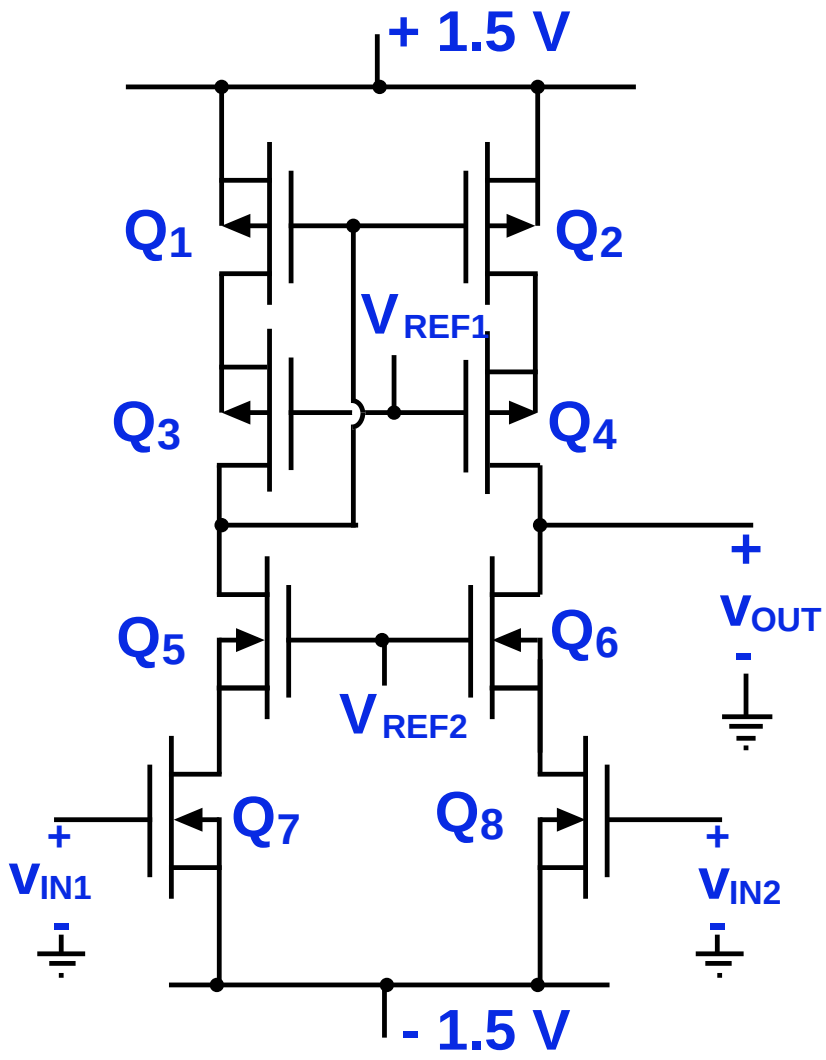


Wilson cascode



The output resistances and load characteristics are identical, but the Wilson load is balanced better in bipolar applications, and the enhanced swing cascode has the largest output voltage swing of any of them.

Specialty pairings: Cascodes in a DP-like amplifier



Comments/Observations:

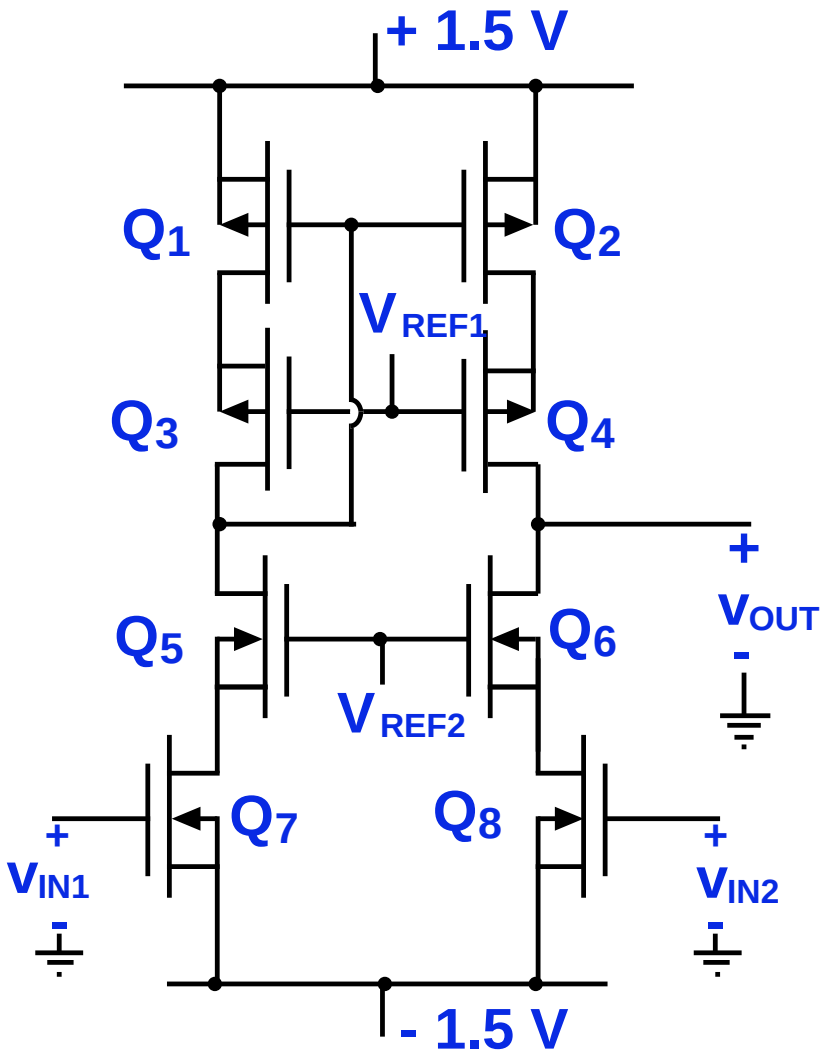
This stage is essentially a normal source-coupled pair with a current mirror load, but there are differences..

The first difference is that two driver transistors are cascode pairs.

The second difference is that the current mirror load is also cascoded.

The third difference is that the stage is not biased with a current source, but is instead biased by the first gain stage.

Specialty pairings: Cascodes in a DP-like amplifier, cont.



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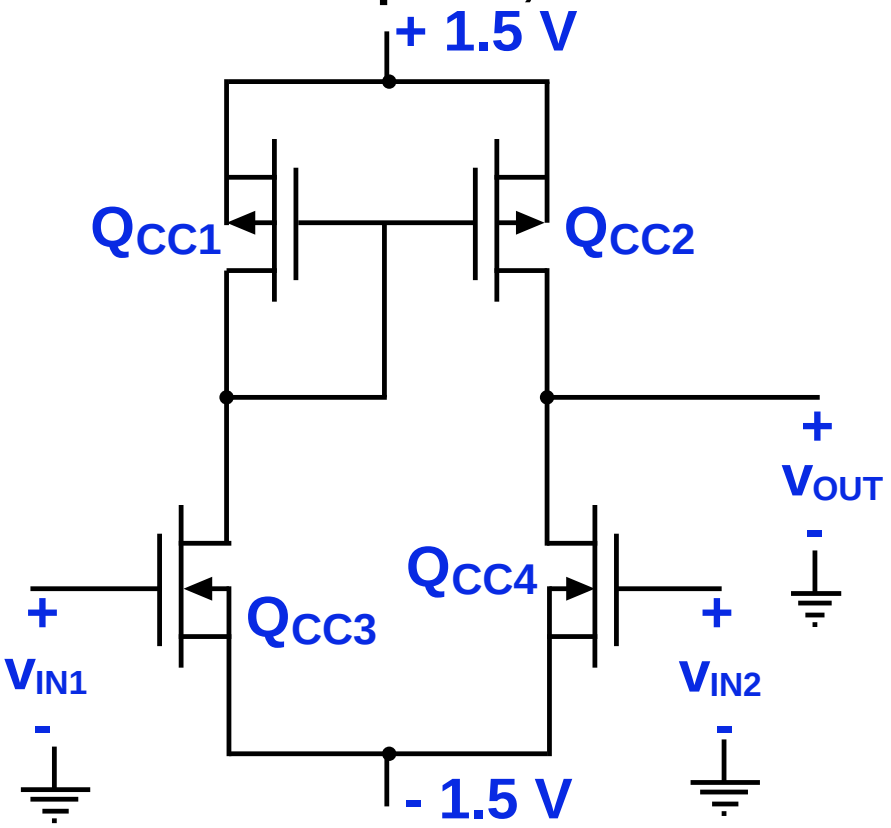


$Q_{CC1} = Q_1/Q_3$

$Q_{CC2} = Q_2/Q_4$

$Q_{CC3} = Q_7/Q_5$

$Q_{CC4} = Q_8/Q_6$

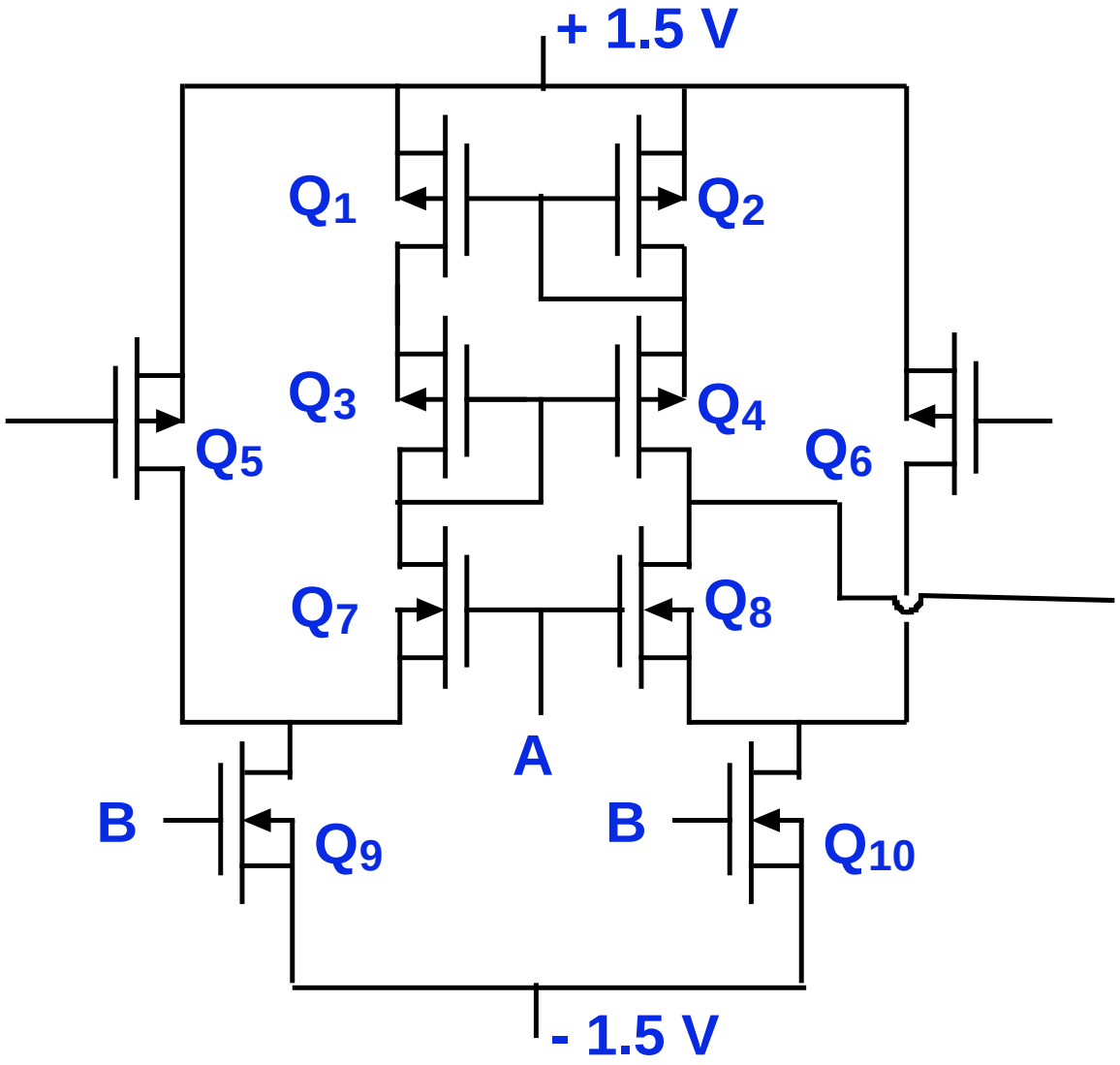
Common sources

Common gates

	$g_{m,CC}$	$g_{o,CC}$
Q_{CC1}	g_{m1}	$g_{o1}g_{o3}/g_{m3}$
Q_{CC2}	g_{m2}	$g_{o2}g_{o4}/g_{m4}$
Q_{CC3}	g_{m7}	$g_{o7}g_{o5}/g_{m5}$
Q_{CC4}	g_{m8}	$g_{o8}g_{o6}/g_{m6}$

Specialty pairings: The Cascode, cont.

The Folded Cascode: another variation



Specialty pairings: The Darlington Connnection

A bipolar pair stage used to get a large input resistance

Input resistance

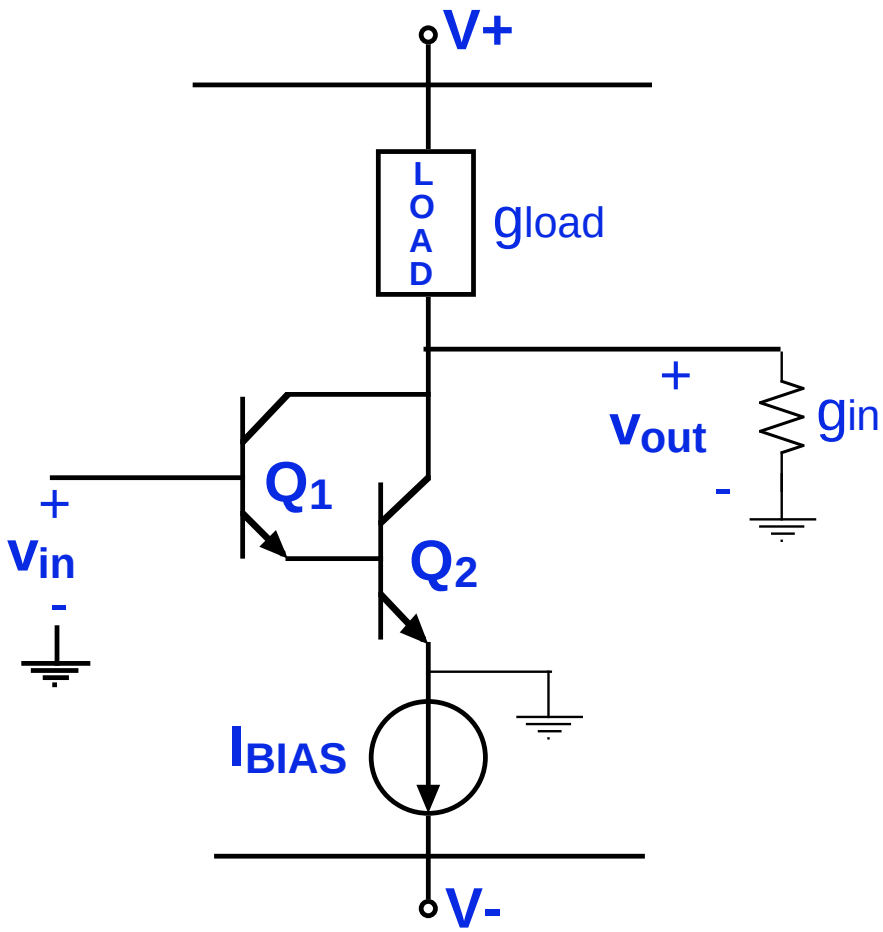
$$r_{in} = 2\beta r_{\pi 2} = 2\beta^2 / g_{m2}$$

Output resistance

$$r_{out} = 1/\left(1.5g_{o2} + g_{load} + g_{in}\right)$$

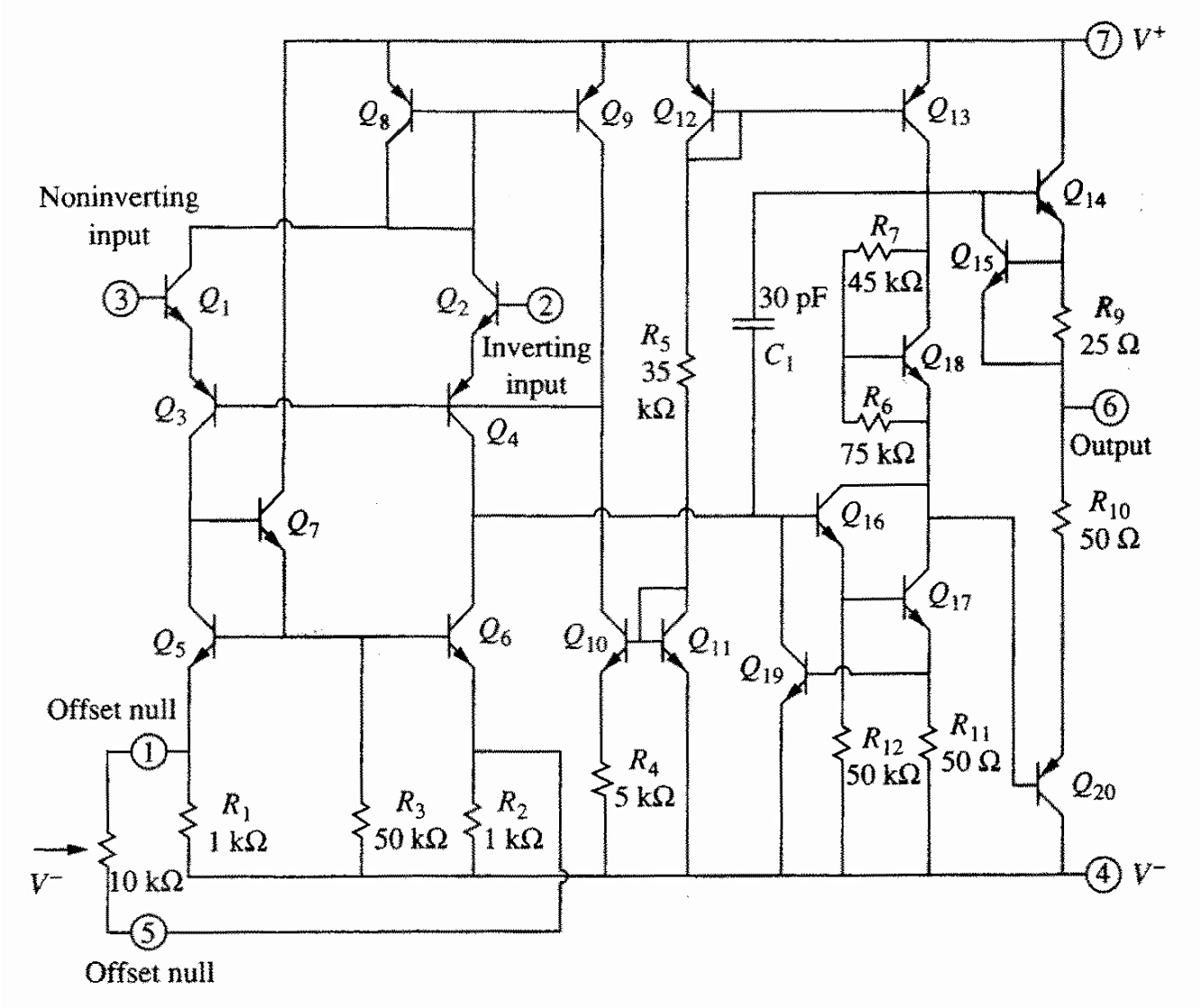
Voltage gain

$$A_v \equiv \frac{v_{out}}{v_{in}} = -\frac{g_{m17}}{2\left(1.5g_{o2} + g_{load} + g_{in}\right)}$$



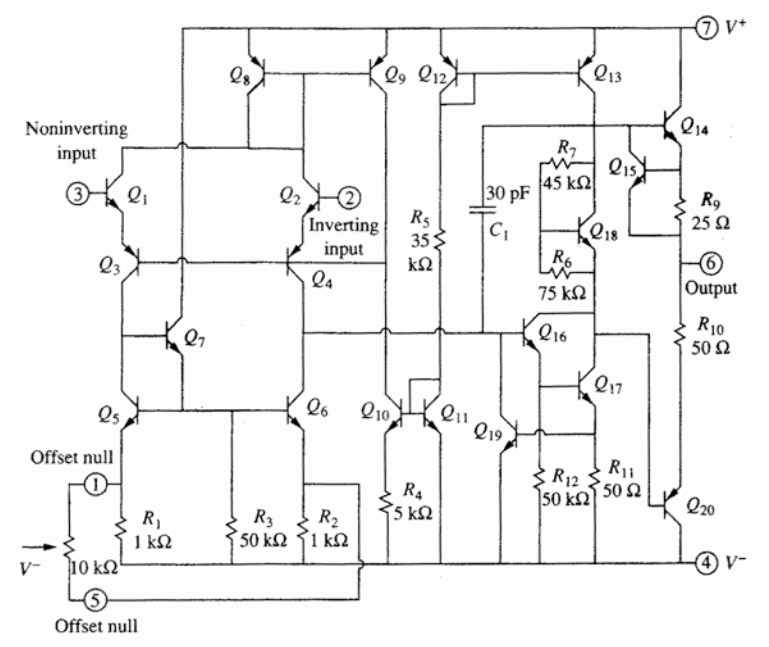
Multi-stage amplifier analysis and design: The μA741

The circuit: a full schematic



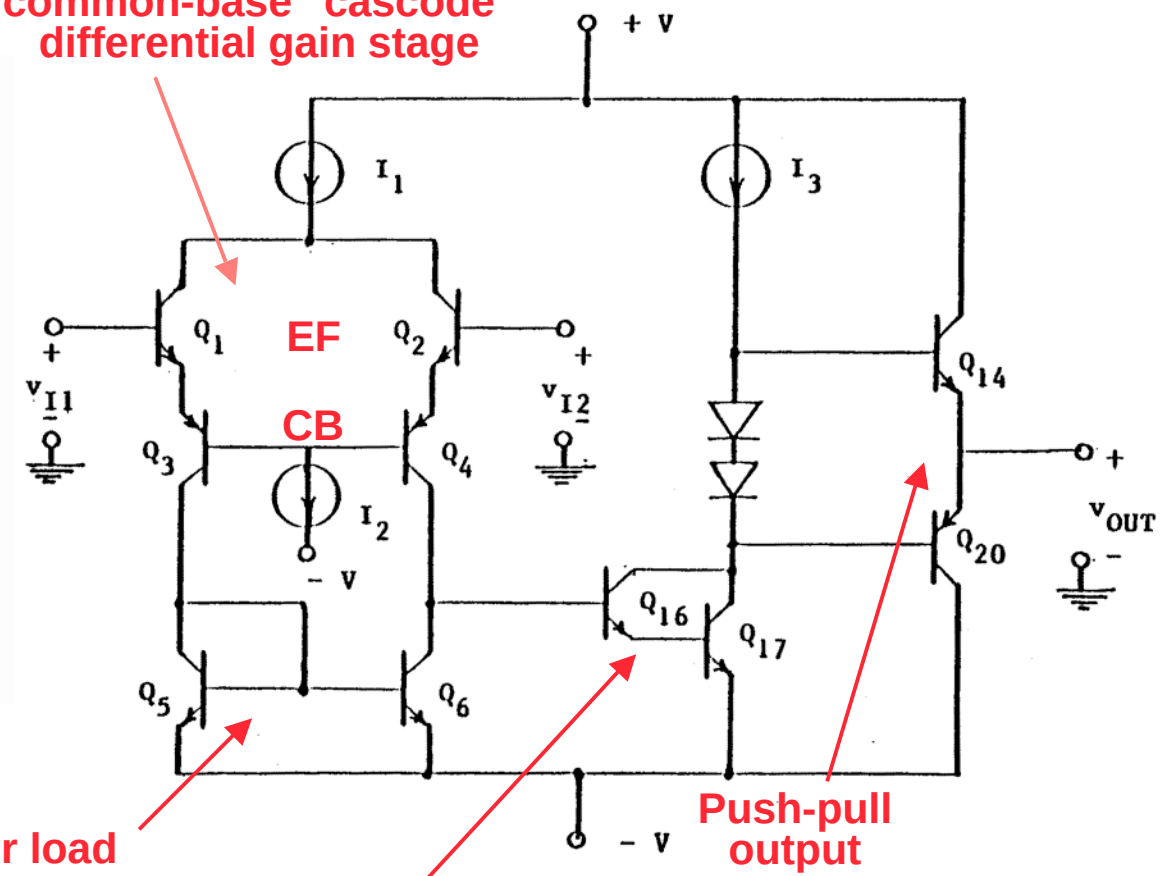
Multi-stage amplifier analysis and design: The μA741

Figuring the circuit out:



The full schematic

Emitter-follower/ common-base "cascode" differential gain stage



Current mirror load

Darlington common-emitter gain stage

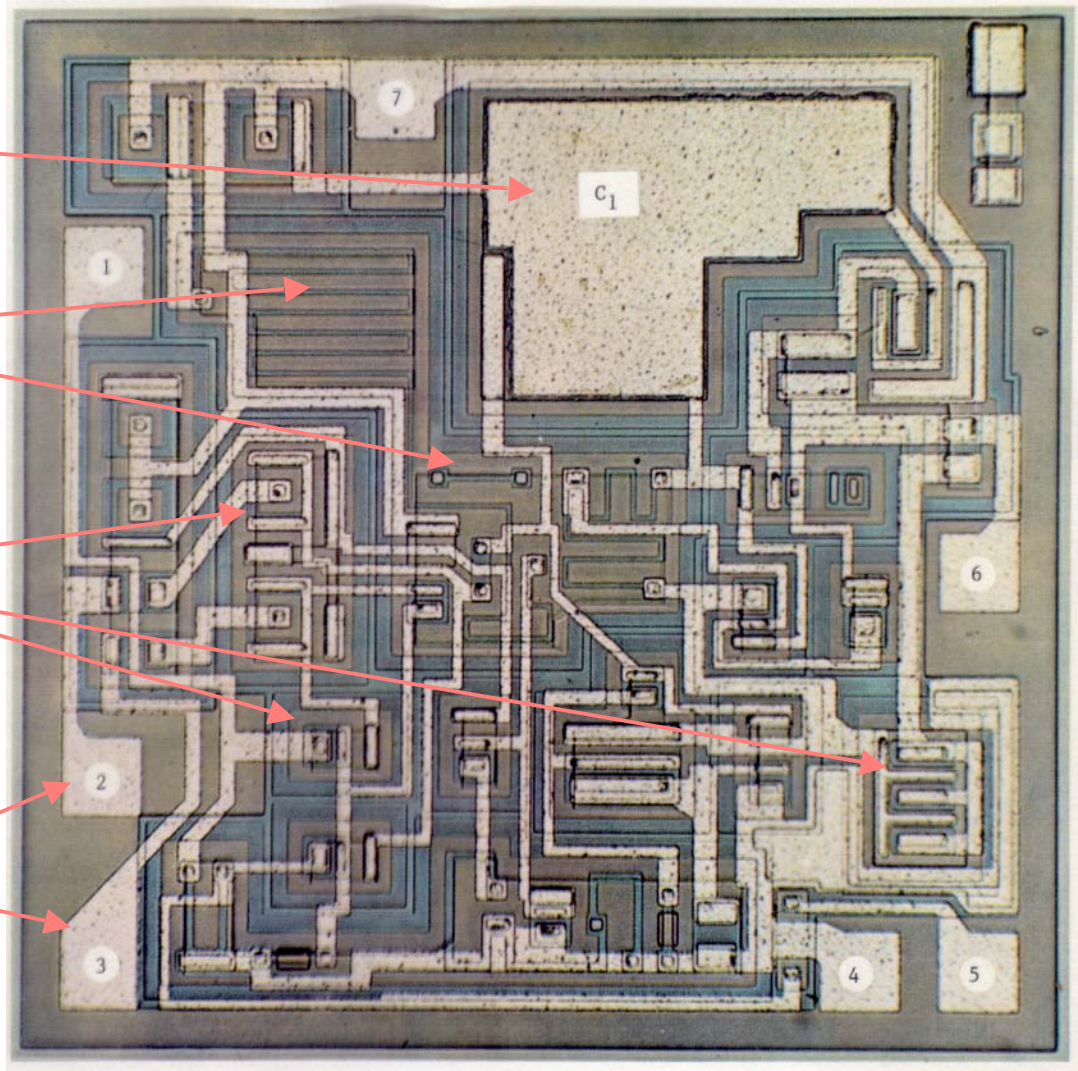
Push-pull output

Simplified schematic

Another interesting discussion of the μA741:
http://en.wikipedia.org/wiki/Operational_amplifier

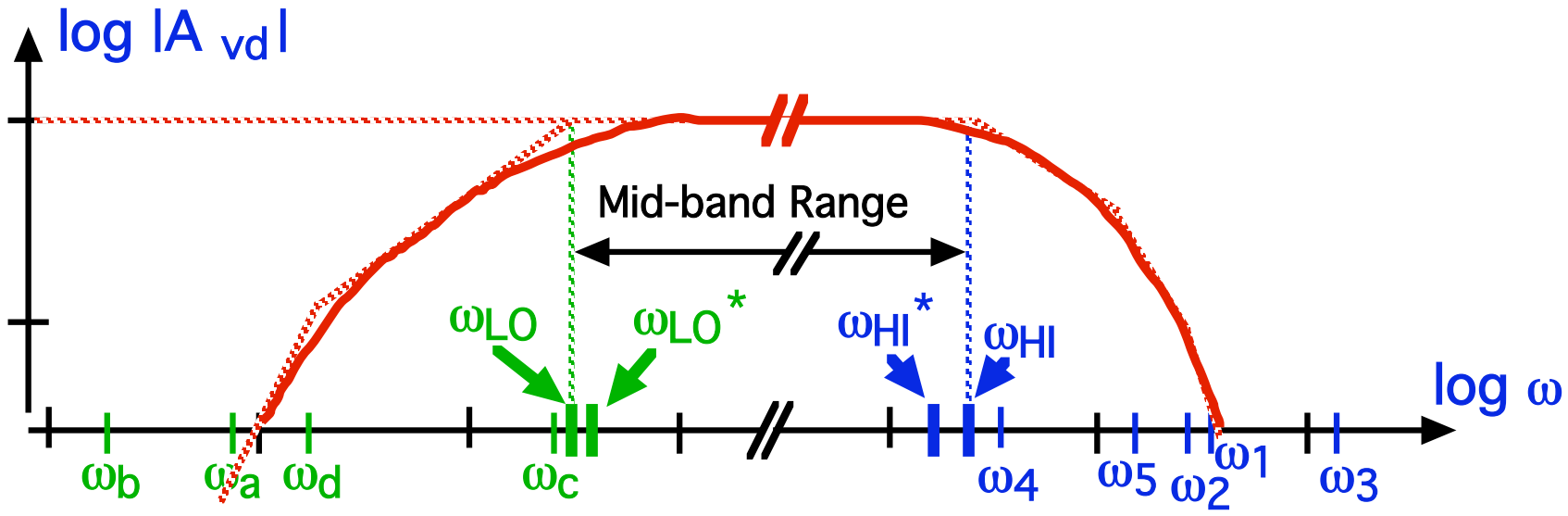
Multi-stage amplifier analysis and design: The μA741

The chip: a bipolar IC



Mid-band, cont: The mid-band range of frequencies

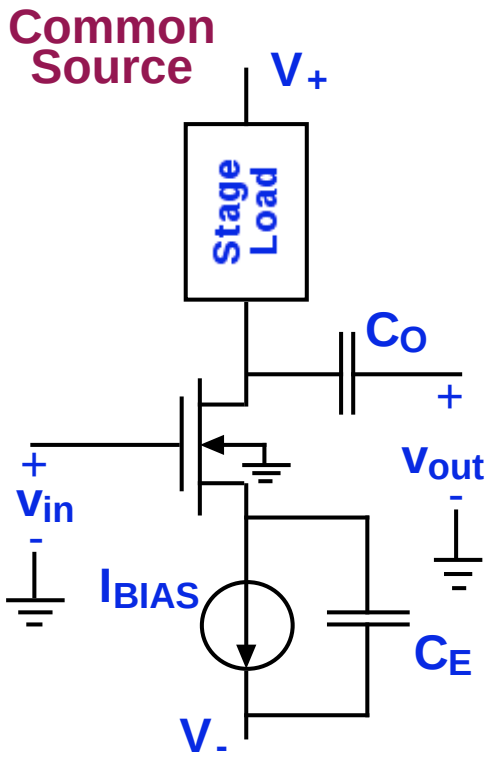
In this range of frequencies the gain is a constant, and the phase shift between the input and output is also constant (either 0° or 180°).

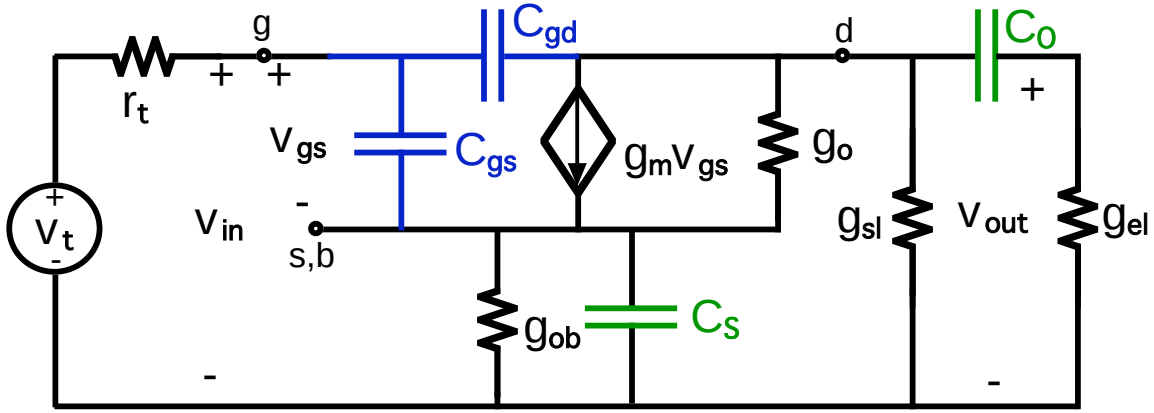


All of the parasitic and intrinsic device capacitances are effectively open circuits

All of the biasing and coupling capacitors are effectively short circuits

Bounding mid-band: frequency range of constant gain and phase



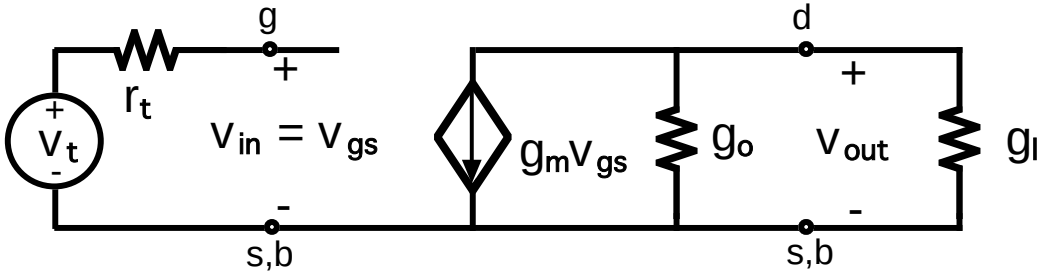


LEC for common source stage with all the capacitors

Biasing capacitors: typically in mF range
(C_O, C_S, etc.) effectively shorts above ω_{LO}

Device capacitors: typically in pF range
(C_{gs}, C_{gd}, etc.) effectively open until ω_{HI}

Mid-band frequencies fall between: $\omega_{LO} < \omega < \omega_{HI}$



Common emitter LEC for in mid-band range Note: $g_l = g_{sl} + g_{el}$

What are ω_{LO} and ω_{HI}?

Estimating ω_{HI} - Open Circuit Time Constants Method

Open circuit time constants (OCTC) recipe:

1. Pick one C_{gd}, C_{gs}, C_{μ}, C_{π}, etc. (call it C_1) and assume all others are open circuits.
2. Find the resistance in parallel with C_1 and call it R_1.
3. Calculate $1/R_1C_1$ and call it ω_1.
4. Repeat this for each of the N different C_{gd}'s, C_{gs}'s, C_{μ}'s, C_{π}'s, etc., in the circuit finding ω_1, ω_2, ω_3, …, ω_N.
5. Define ω_{HI}* as the inverse of the sum of the inverses of the N ω_i's:

$$\omega_{HI}^* = [\Sigma(\omega_i)^{-1}]^{-1} = [\Sigma R_i C_i]^{-1}$$

6. The true ω_{HI} is similar to, but greater than, ω_{HI}*.

Observations:

The OCTC method gives a conservative, low estimate for ω_{HI}.

The sum of inverses favors the smallest ω_i, and thus the capacitor with the largest RC product dominates ω_{HI}*.

Estimating ω_{LO} - Short Circuit Time Constants Method

Short circuit time constants (SCTC) recipe:

1. Pick one C_O, C_I, C_E, etc. (call it C_1) and assume all others are short circuits.
2. Find the resistance in parallel with C_1 and call it R_1.
3. Calculate $1/R_1C_1$ and call it ω_1.
4. Repeat this for each of the M different C_I's, C_O's, C_E's, C_S's, etc., in the circuit finding ω_1, ω_2, ω_3, …, ω_M.
5. Define ω_{LO}^* as the sum of the M ω_j's:

$$\omega_{LO}^* = [\Sigma(\omega_j)] = [\Sigma(R_jC_j)^{-1}]$$

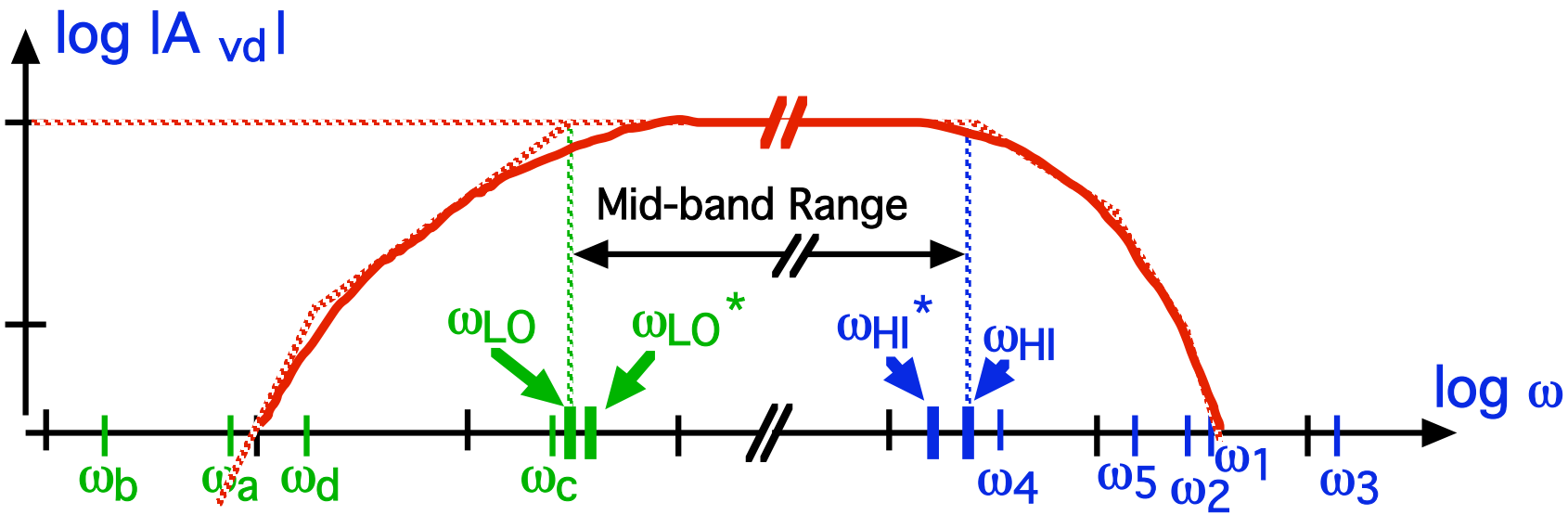
6. The true ω_{LO} is similar to, but less than, ω_{LO}^*.

Observations:

The SCTC method gives a conservative, high estimate for ω_{LO}.

The sum of inverses favors the largest ω_j, and thus the capacitor with the smallest RC product dominates ω_{LO}^*.

Summary of OCTC and SCTC results



- **OCTC:** an estimate for ω_{HI}
  1. ω_{HI}* is a weighted sum of ω's associated with device capacitances: (add RC's and invert)
  2. Smallest ω (largest RC) dominates ω_{HI}*
  3. Provides a lower bound on ω_{HI}
- **SCTC:** an estimate for ω_{LO}
  1. ω_{LO}* is a weighted sum of w's associated with bias capacitors: (add ω's directly)
  2. Largest ω (smallest RC) dominates ω_{LO}*
  3. Provides a upper bound on ω_{LO}

Lecture 22 - Diff-Amp Analysis II - Summary

- **Design Problem Issues**
  - **Q13, Q13'; voltage gains**
- **Specialty stages - useful pairings**
  - **Source coupled pairs:** MOS
  - **Push-pull output:** Two followers in vertical chain
    - Very low output resistance
    - Shared duties for positive and negative output swings
  - **Cascode:** Common-source/emitter performance
    - Greatly enhanced output resistance
    - Find greatly enhanced high frequency performance also
  - **Darlington:** Increased input resistance ona bipolar stage
  - **µA 741:** A workhorse IC showing all of these pairs
- **Bounding mid-band**
  - **Open Circuit Time Constant Method:** An estimate of ω_{HI}
  - **Short Circuit Time Constant Method:** An estimate of ω_{LO}

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