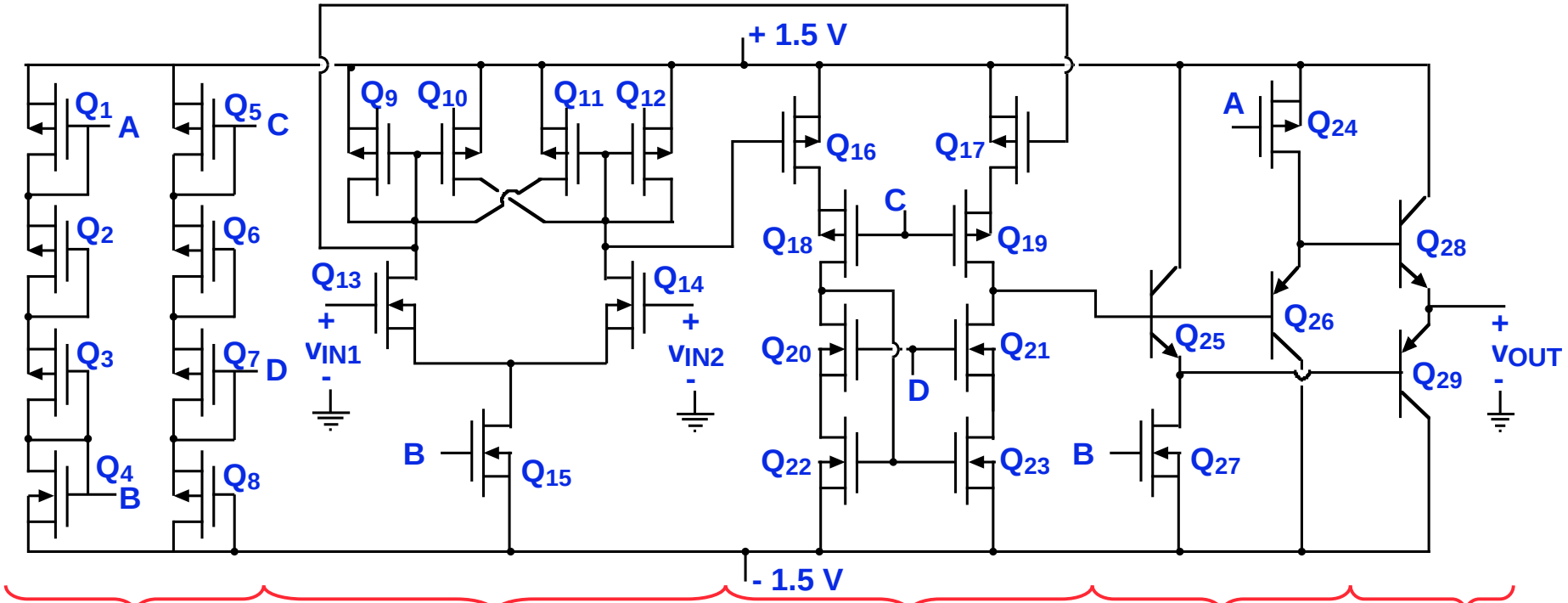
6.012 - Microelectronic Devices and Circuits

Spring 2006 Design Problem Circuit

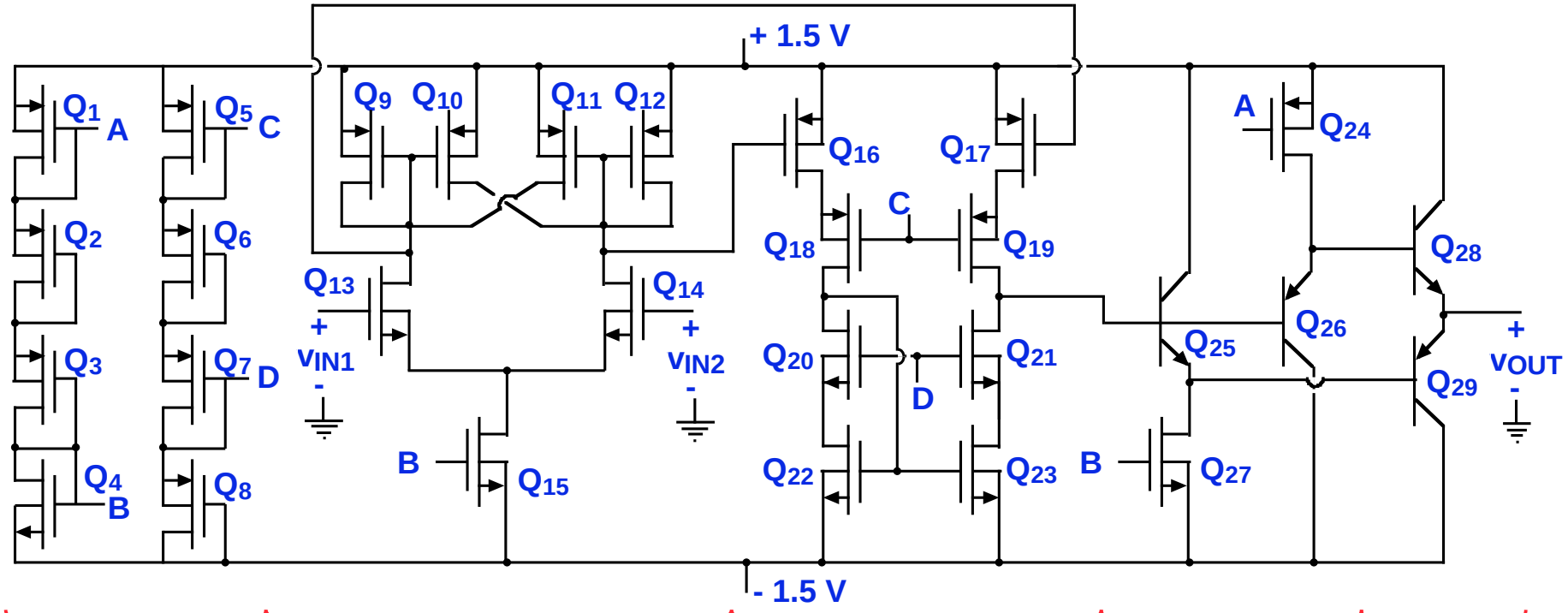
Full schematic



*** Common source stage followed by common base stage.**

Circuit drawn with alternative MOSFET symbols:

Some find the MOSFET symbols used in this version of the schematic with the arrow on the source, rather than the gate, more intuitive when looking at a schematic. The rest of the foils in this set use the original symbols, so this figure help you adapt those foils if you prefer these alternative symbols.



Bias chains

Source-coupled pair gain stage with Lee active load

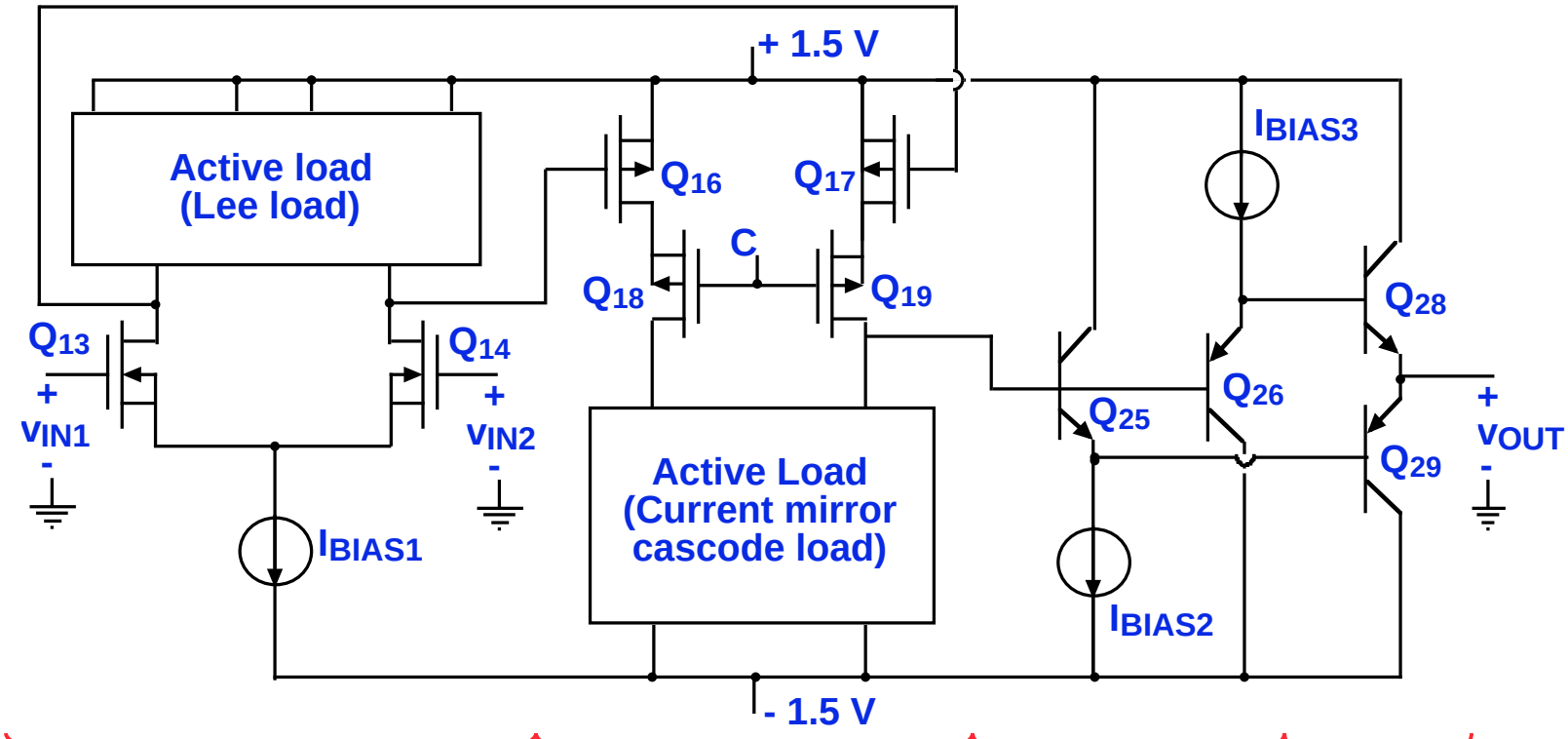
Cascode* differential gain stage with cascode current mirror active load

Complementary emitter-follower output stages

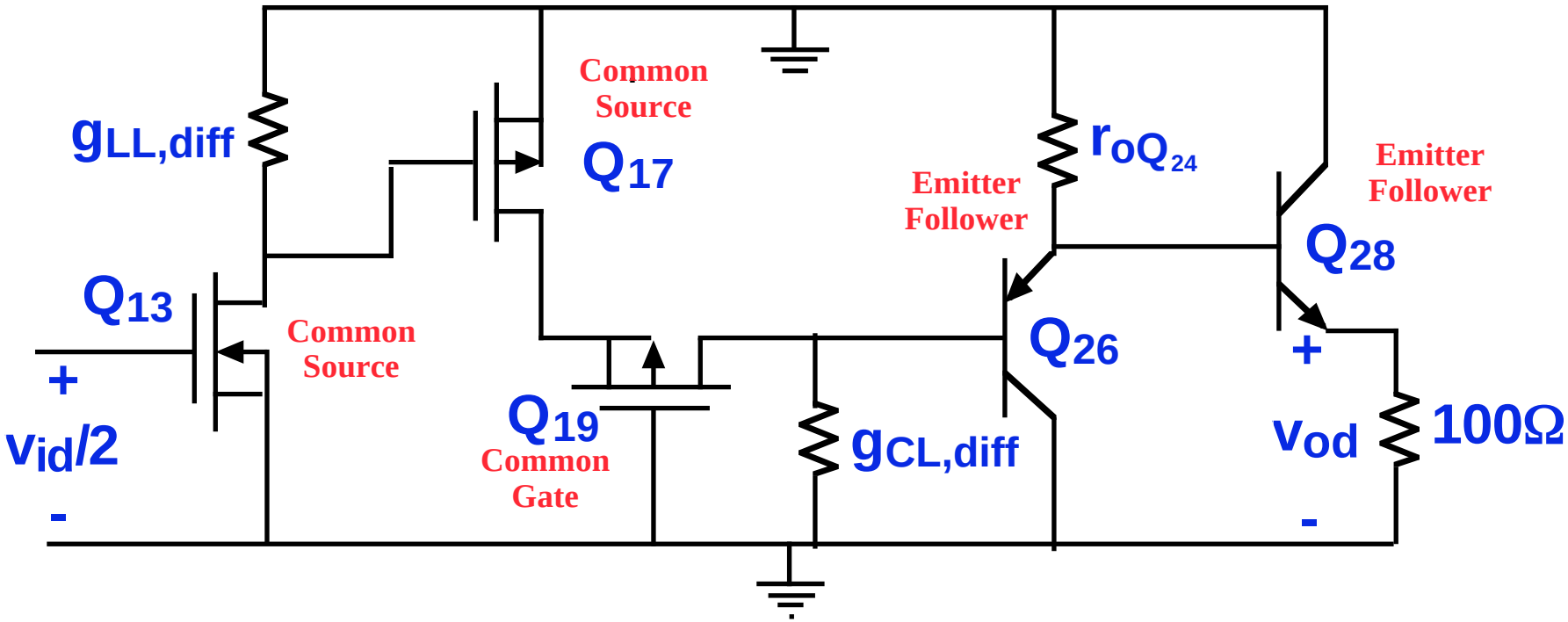
Push-pull output stage

•Common source stage followed by common base stage.

Conceptual schematic: full circuit

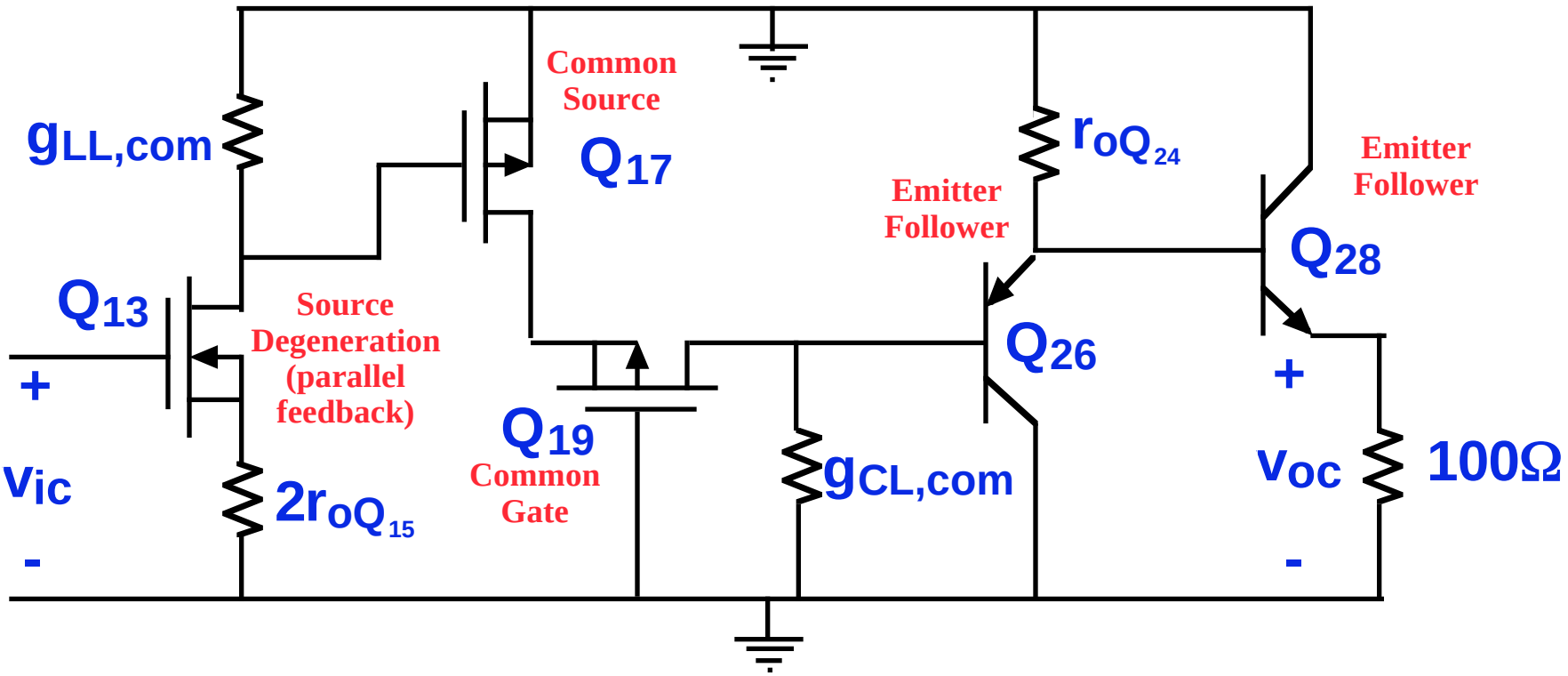


Conceptual schematic: difference-mode inputs



$$A_{vd} = v_{od}/v_{id}$$

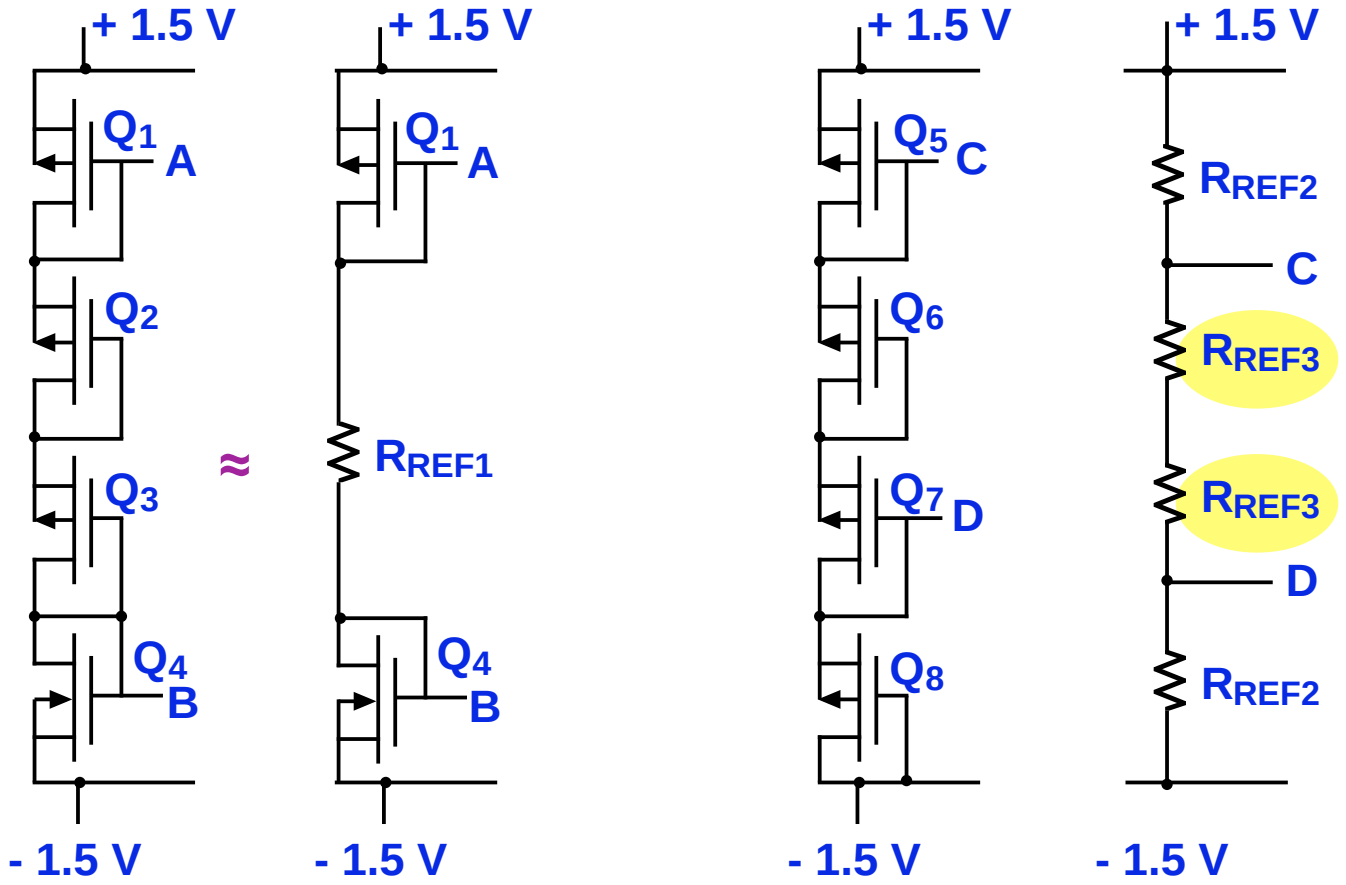
Conceptual schematic: common-mode inputs



$$A_{vc} = v_{oc}/v_{ic}$$

Left to right through the design problem circuit:

1. **Biasing: the bias chains**

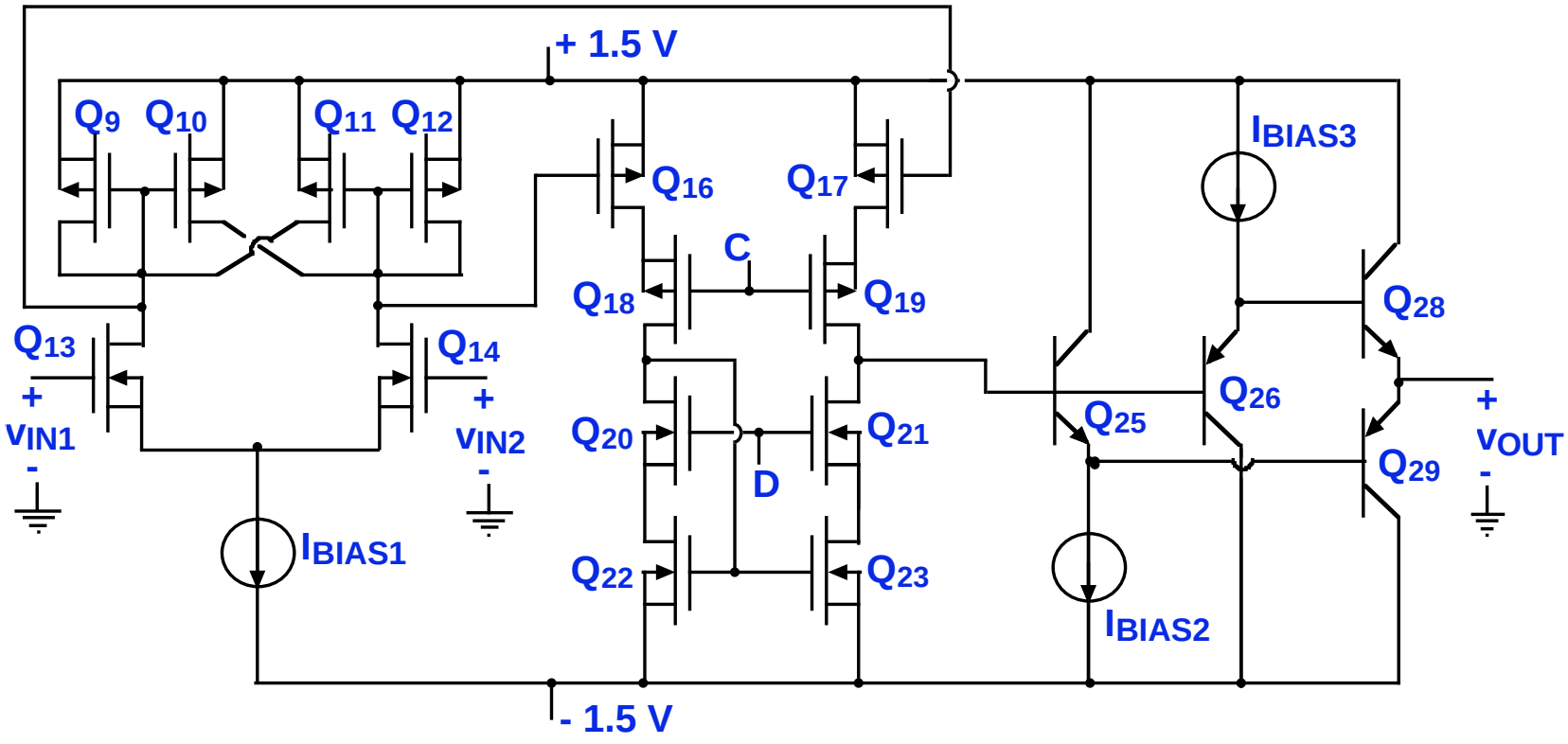


Points to ponder:

- What is the drain current of a minimum size n-channel MOSFET when $(V_{GS}-V_T) = (V_{GS}-V_T)_{min}$? What is it for a minimally biased p-channel MOSFET?
- How can Q_1 and Q_4 both be at this minimum bias point?

Left to right through the design problem circuit:

1. **Biasing: looking at how each of the four stages is biased**



Stage 1: Biased by the current source, I_{BIAS1}

Stage 2: Biased by Q_9, Q_{10}, Q_{11}, and Q_{12}.

Stage 3: Biased by I_{BIAS2} and I_{BIAS3}.

Stage 4: Biased by Q_{25} and Q_{26}.

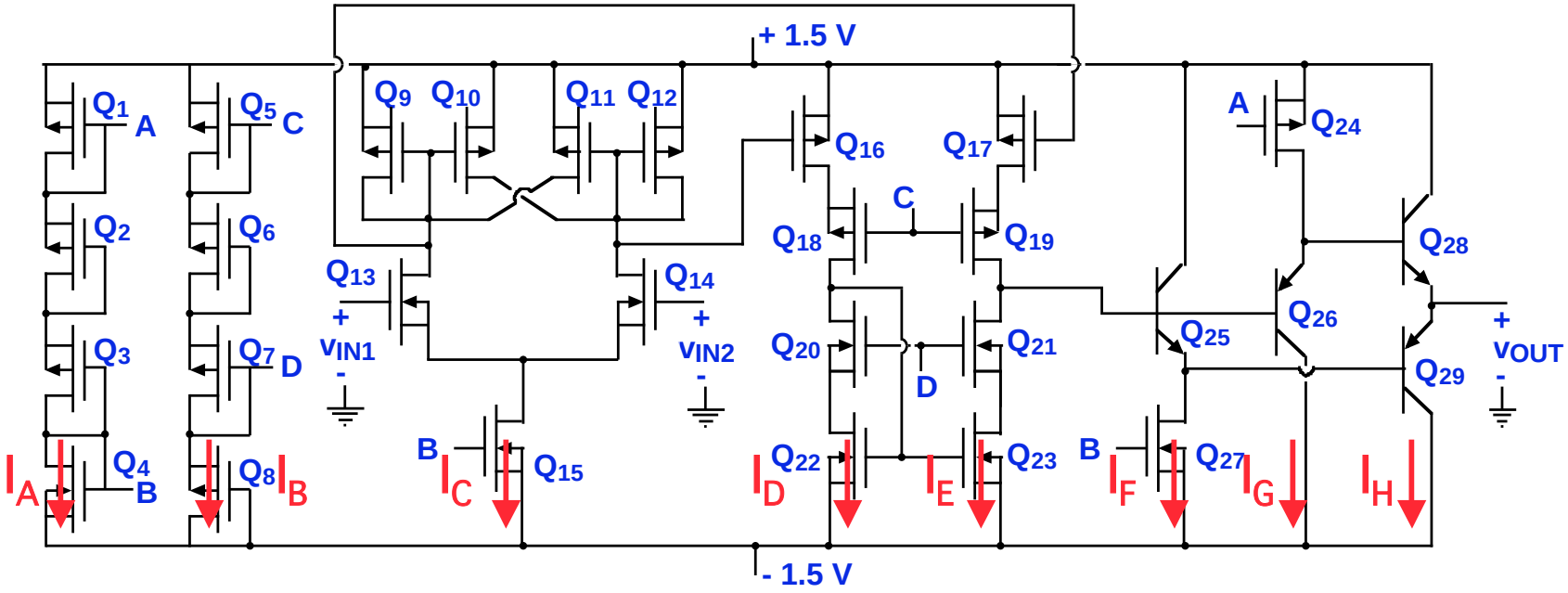
Point to ponder:

- **Stages 2 and 4 are biased by the preceding stages.**

Left to right through the design problem circuit:

1. **Biasing: power dissipation**

A constraint on the bias currents is the total power dissipation specification of 7.5 mW. This means that the total bias current must be less that 2.5 mA (i.e, 3 V x 2.5 mA = 7.5 mW).



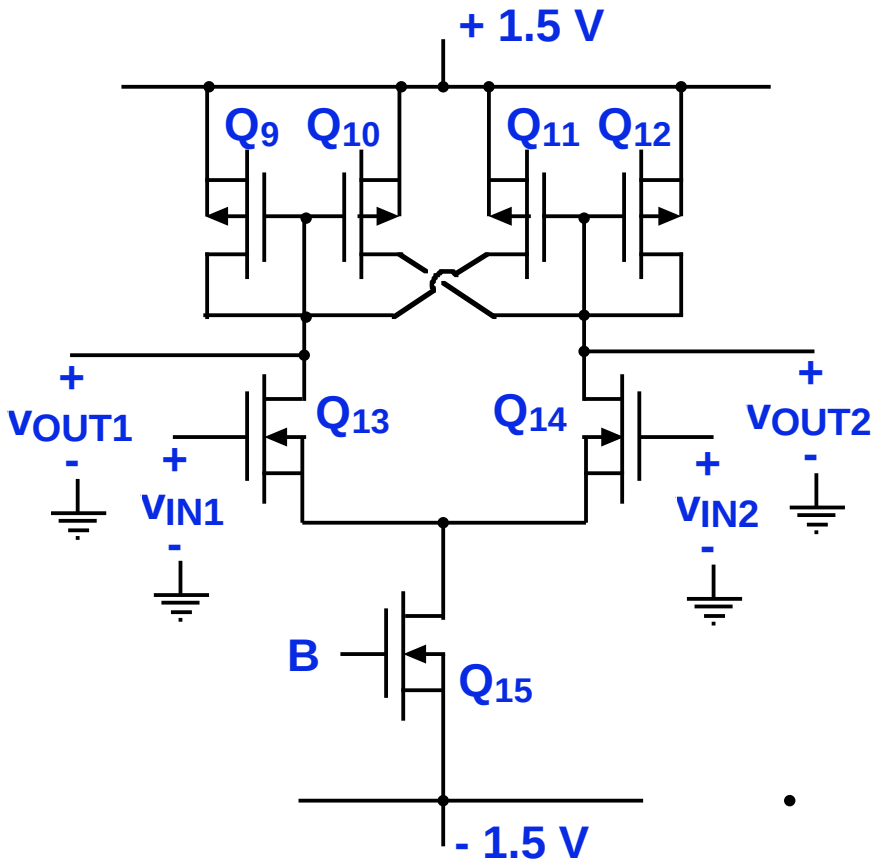
$$I_A + I_B + I_C + I_D + I_E + I_F + I_G + I_H \leq 2.5\ mA$$

$$P_Q = \left(I_A + I_B + I_C + I_D + I_E + I_F + I_G + I_H\right) \times 3\ Volts$$

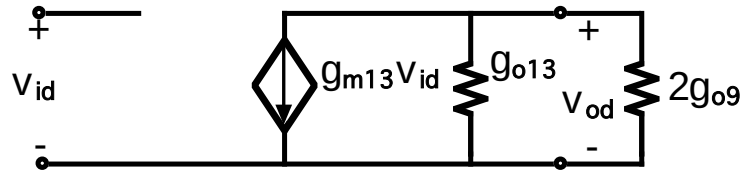
Left to right through the design problem circuit:

2. **First gain stage: gain of source-coupled pair with Lee load**

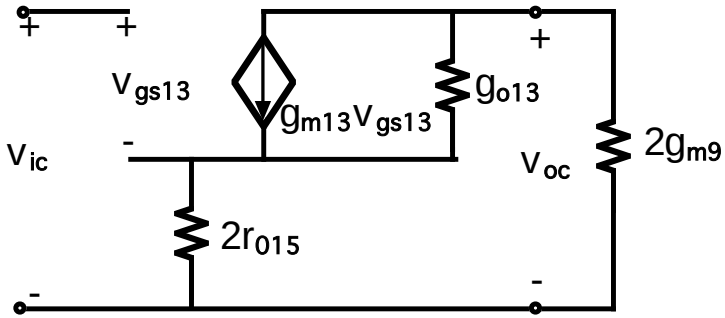
A Lee Load is an active load that looks different in common and difference mode. A full analysis can be found in the handout "Two Active Loads" posted on Stellar.



Difference mode:



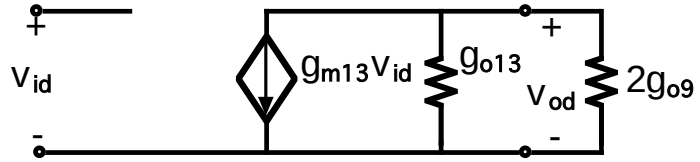
Common mode:



Left to right through the design problem circuit:

2. First gain stage: gain of source-coupled pair with Lee load

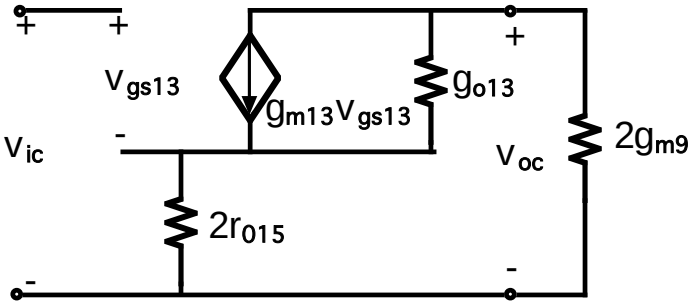
Difference mode:



$$v_{od} = \frac{-g_{m13}}{g_{013} + 2g_{09}} v_{id}$$

$$= \frac{2I_{D13}}{\frac{(V_{GS13} - V_{Tn})}{I_{D13}} + 2\frac{I_{D13}/2}{V_{A9}}} v_{id} = \frac{2\left(\frac{V_{A9}V_{A13}}{V_{A9} + V_{A13}}\right)}{(V_{GS13} - V_{Tn})} v_{id} = \frac{2V_{A,eff\,9,13}}{(V_{GS13} - V_{Tn})} v_{id}$$

Common mode:



$$v_{oc} \approx \frac{-g_{015}}{4g_{m9}} v_{ic} = \frac{(V_{GS9} - V_{Tp})}{2V_{A15}} v_{ic}$$

Combined:

$$v_{out1} = \frac{-g_{m13}}{g_{o13} + 2g_{o9}} \cdot \frac{(v_{in1} - v_{in2})}{2} - \frac{g_{015}}{4g_{m9}} \cdot \frac{(v_{in1} + v_{in2})}{2} = \frac{-V_{A.eff\,9,13}}{(V_{GS13} - V_{Tn})} \cdot (v_{in1} - v_{in2}) - \frac{(V_{GS13} - V_{Tn})}{2V_{A15}} \cdot \frac{(v_{in1} + v_{in2})}{2}$$

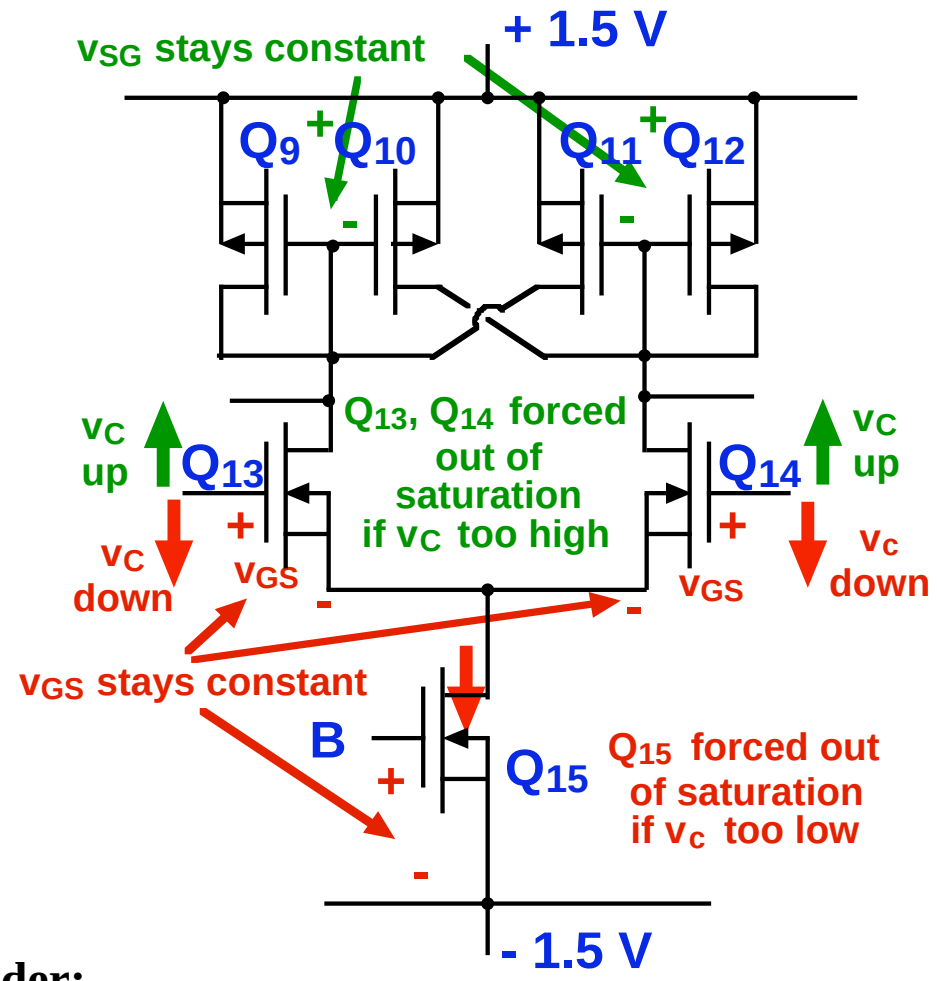
$$v_{out2} = \frac{g_{m13}}{g_{o13} + 2g_{o9}} \cdot \frac{(v_{in1} - v_{in2})}{2} - \frac{g_{015}}{4g_{m9}} \cdot \frac{(v_{in1} + v_{in2})}{2} = \frac{V_{A.eff\,9,13}}{(V_{GS13} - V_{Tn})} \cdot (v_{in1} - v_{in2}) - \frac{(V_{GS13} - V_{Tn})}{2V_{A15}} \cdot \frac{(v_{in1} + v_{in2})}{2}$$

Points to ponder:

- **The outputs go to the gates of other MOSFET, so they do not load this stage. What does this about getting the maximum difference mode out of this stage?**
- **How can Q_9 through Q_{15} all be biased at their minimum bias point?**

Left to right through the design problem circuit:

2. First gain stage, cont: common-mode input range

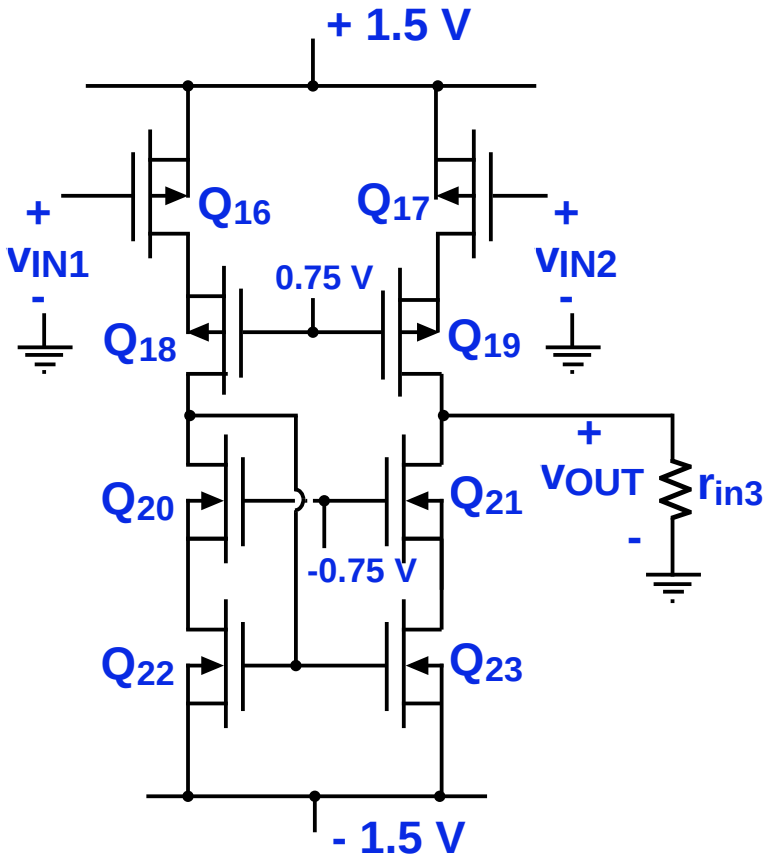


Point to ponder:

- What is v_{DS} and what is v_{GD} at the boundary between the saturation and linear regions?

Left to right through the design problem circuit:

3. Second gain stage: source-coupled cascode, current mirror load



Comments/Observations:

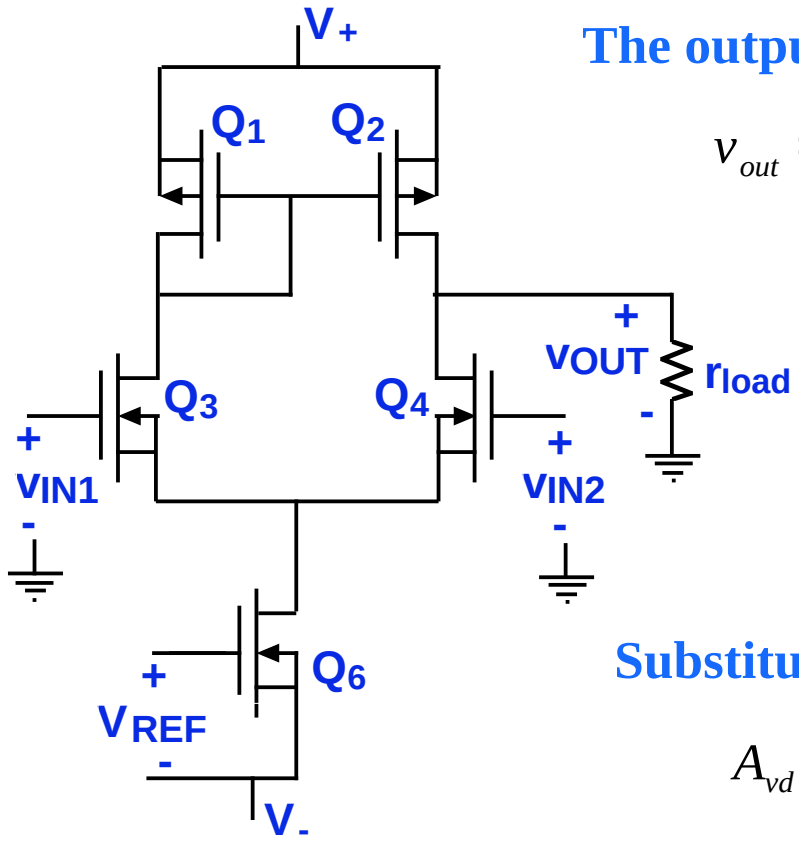
- This stage is essentially a normal source-coupled pair with a current mirror load, but there are differences..
- The first difference is that two driver transistors are cascode pairs. The stage thus has two sub-stages, the first being a source-coupled pair which is loaded by the second, which is a common-gate pair. The combination of a common source stage followed by a common gate stage is called a "cascode.
- The second difference is that the current mirror load is also cascoded.
- The third difference is that the stage is not biased with a current mirror, but is instead biased by the first gain stage.

Point to ponder:

- Notice that output of the stage is loaded by the input resistance of the third stage. In the first stage there was no loading. How does this effect the gain and how we maximize it?

Left to right through the design problem circuit:

3. Second stage: gain of a simple current mirror with loading



The output voltage is, in general:

$$v_{out} = \frac{g_{m3}}{g_{01} + g_{03} + g_{load}}(v_1 - v_2) + \frac{g_{06}}{2g_{m3}}(v_1 + v_2)$$

Focusing on the differential gain and writing it in terms of the bias point:

$$A_{vd} = \frac{g_{m3}}{g_{01} + g_{03} + g_{load}} = \frac{K_3(V_{GS3} - V_{TN})}{(I_D / V_{A,eff}) + g_{load}}$$

Substituting for I_D and dividing by K_3:

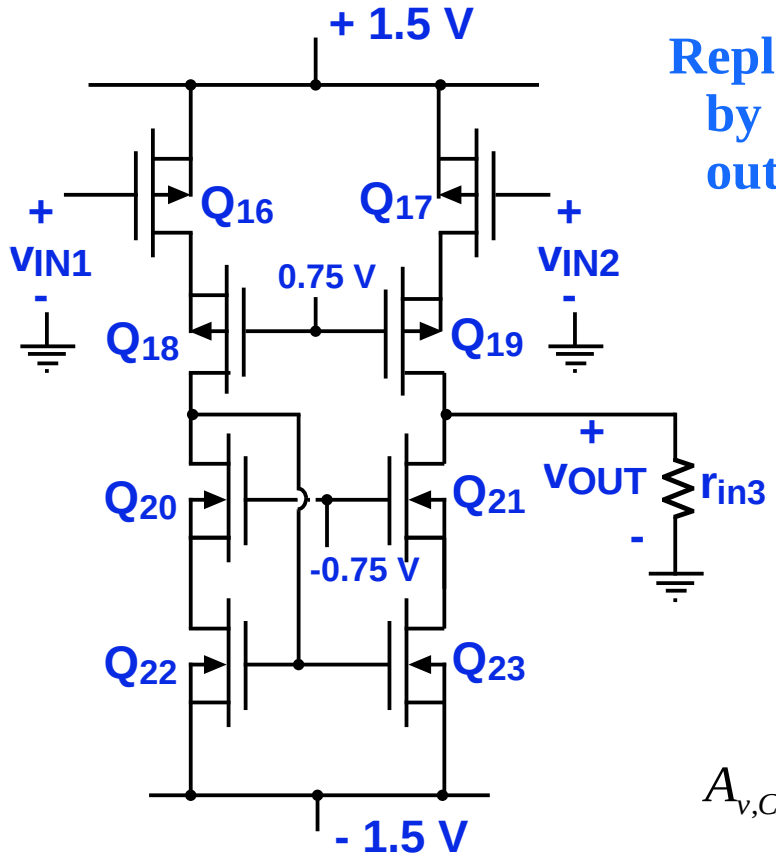
$$A_{vd} = \frac{(V_{GS3} - V_{TN})}{\left[\frac{(V_{GS3} - V_{TN})^2}{2V_{A,eff}} + \frac{g_{load}}{K_3}\right]}$$

Point to ponder:

- When the output is not loaded the voltage gain, $2V_{A,eff}/(V_{GS3} - V_{TN})$, does not depend on the K's of the transistors, but when it is loaded by r_{load}, making K bigger can increase the gain.

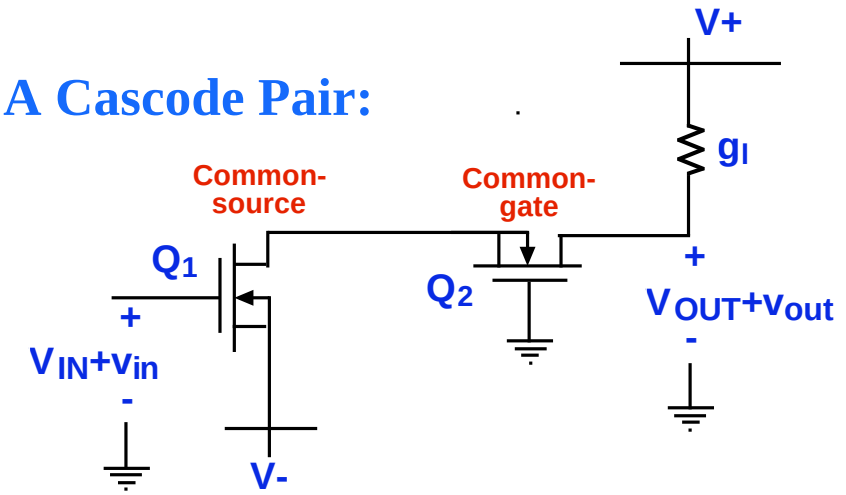
Left to right through the design problem circuit:

3. Second stage: the impact of having cascode pairs



Replacing all the transistors in a current mirror by cascode pairs significantly increases the output resistances and the maximum gain:

A Cascode Pair:



$$A_{v,Cascode} = \frac{v_{out}}{v_{in}} = -\frac{g_{m1}}{g_l + g_{02}\dfrac{g_{01}}{g_{m2}}}, \qquad r_{out} = r_{01}\frac{g_{m2}}{g_{02}}$$

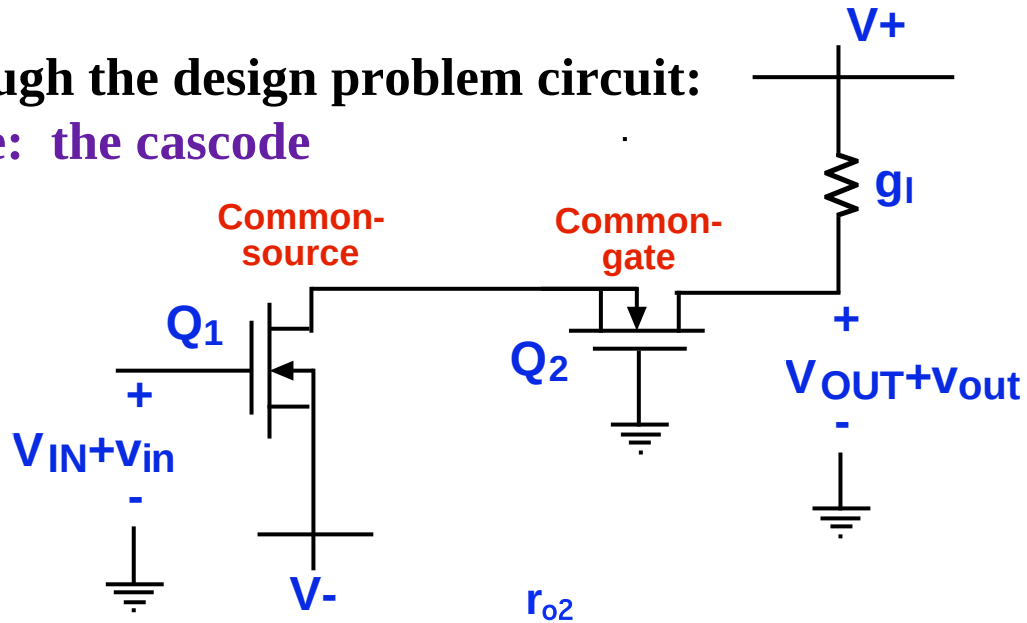
Points to ponder:

- What is the value of g_{load}?
- Is it feasible to bias Q_{16} and Q17 to get the largest gain? How close can one come?
- Changing the bias on Q_{16}/Q_{17} means that of $Q_9/Q_{10}/Q_{11}/Q_{12}$ must change. Is this OK?
- How much can K be increased? Is there any disadvantage to making K this big?
- Over what range can v_{OUT} swing (positive and negative)?

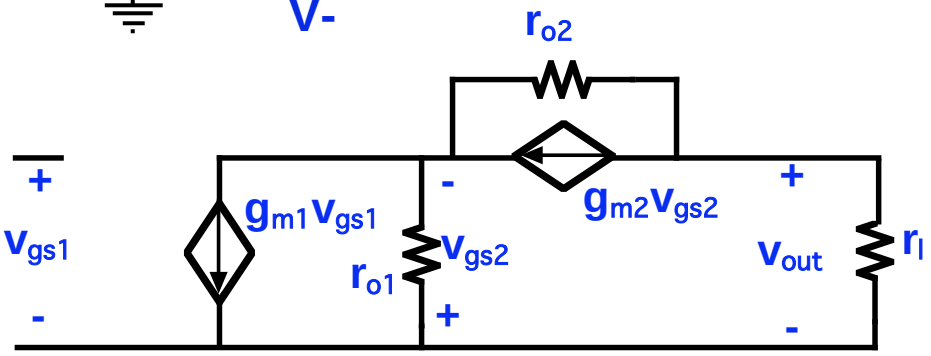
Left to right through the design problem circuit:

3. Second stage: the cascode

Schematic:



L.E.C.:



$$A_v = \frac{v_{out}}{v_{in}} = \frac{-g_{m1}}{g_l + \frac{g_{01}}{(g_{m2}+g_{02})}(g_l + g_{02})} \approx_o \frac{-g_{m1}}{g_l + g_{01}\frac{g_{02}}{g_{m2}}}$$

$$r_{out} = \frac{g_{m2} + g_{02} + g_{01}}{g_{02}g_{01}} \approx r_{01}\frac{g_{m2}}{g_{02}}$$

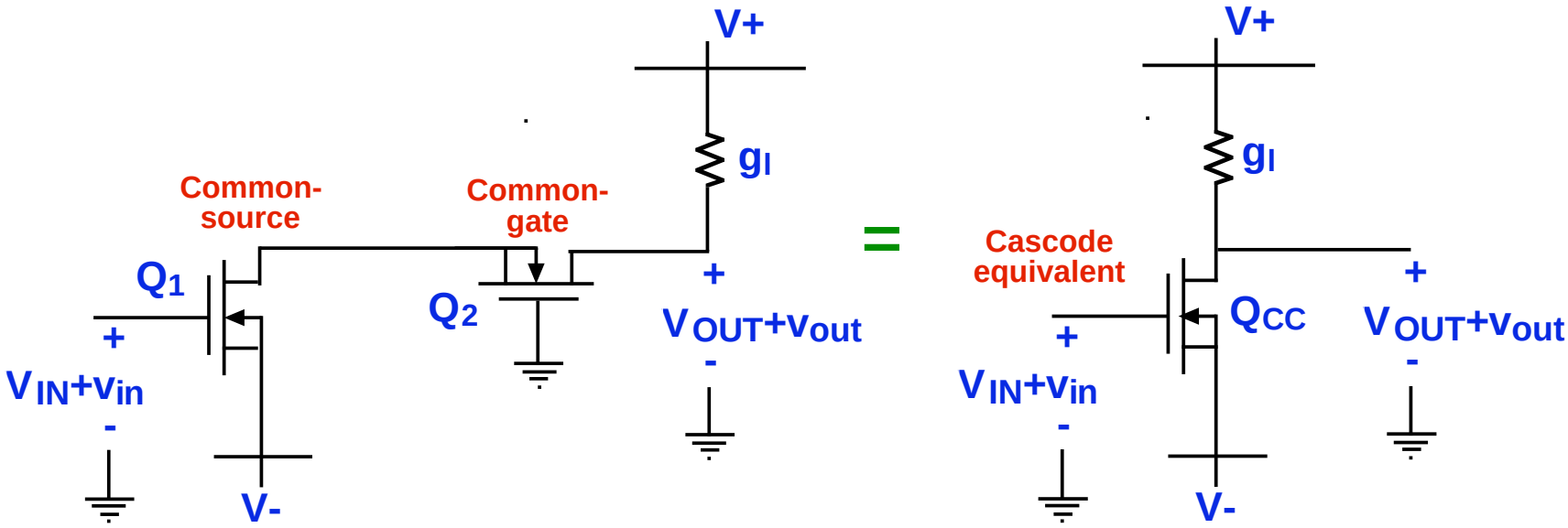
Point to ponder:

- **A_v of a common-source stage, with a much larger output resistance.**

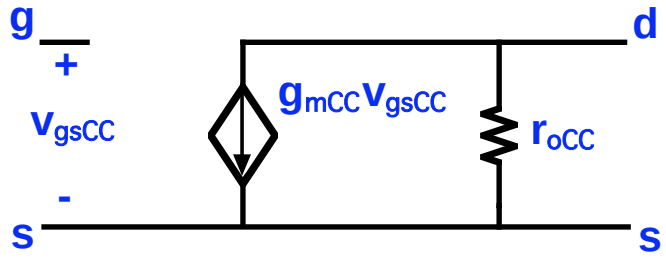
Left to right through the design problem circuit:

3. Second stage: looking more at the cascode

The cascode stage looks like a common source stage made of a special "cascode" transistor, Q_{CC}:



Q_{CC}:

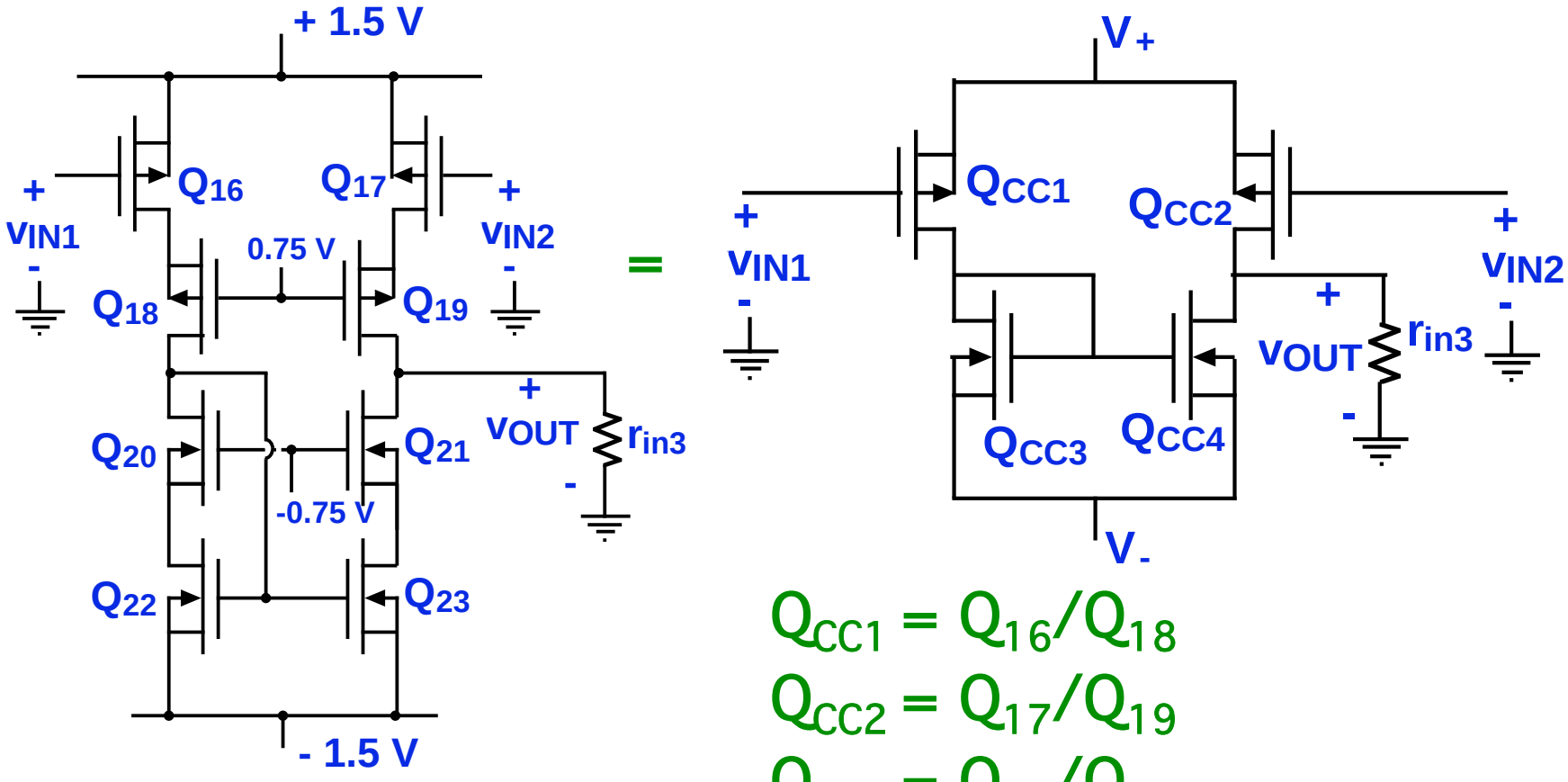


$$g_{m,CC} = g_{m1} \qquad r_{o,CC} \approx r_{01}\frac{g_{m2}}{g_{o2}}$$

$$V_{A,CC} \approx V_{A1}\frac{g_{m2}}{g_{o2}} \quad \text{or} \quad \lambda_{CC} = \lambda_1\frac{g_{o2}}{g_{m2}}$$

Left to right through the design problem circuit:

3. Second gain stage: substituting the cascode equivalents



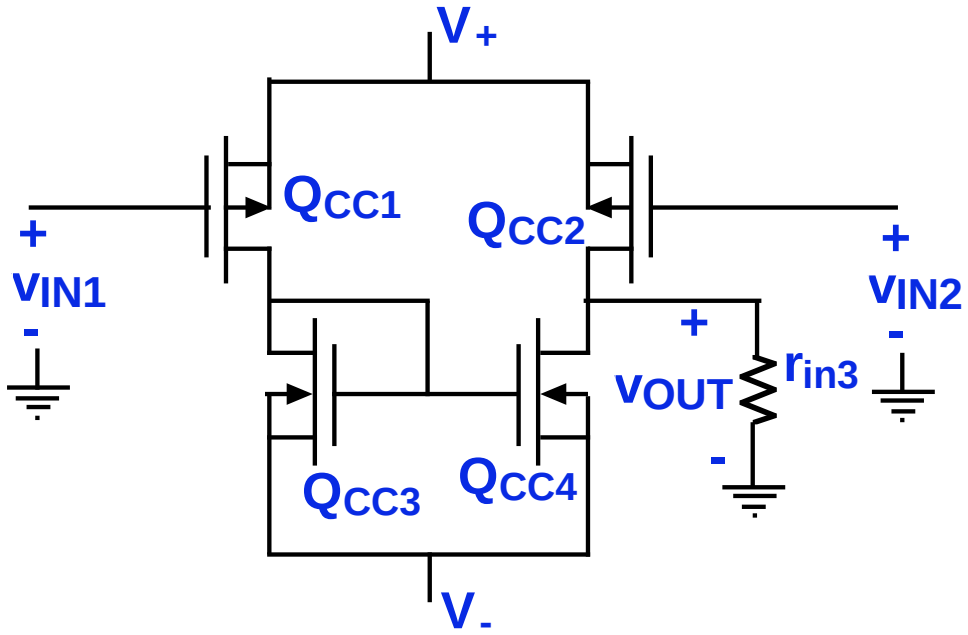
$$Q_{CC1} = Q_{16}/Q_{18}$$
$$Q_{CC2} = Q_{17}/Q_{19}$$
$$Q_{CC3} = Q_{22}/Q_{20}$$
$$Q_{CC4} = Q_{23}/Q_{21}$$

Common source

Common gate

Left to right through the design problem circuit:

3. Second gain stage: substituting the cascode equivalents



	$g_{m,CC}$	$g_{o,CC}$
Q_{CC1}	g_{m16}	$g_{o16}g_{o18} / g_{m18}$
Q_{CC2}	g_{m17}	$g_{o17}g_{o19} / g_{m19}$
Q_{CC3}	g_{m22}	$g_{o22}g_{o20} / g_{m20}$
Q_{CC4}	g_{m23}	$g_{o23}g_{o21} / g_{m21}$

$$v_{out} = A_{vd}v_{id} + A_{vc}v_{ic} = A_{vd}\left(v_{in1} - v_{in2}\right) + A_{vc}\frac{\left(v_{in1} + v_{in2}\right)}{2}$$

$A_{vd} = v_{out}/(v_{in1}-v_{in2})$ with $v_{in1} = v_{id}/2$, $v_{in2} = -v_{id}/2$:

$$A_{vd} = \frac{2g_{m,CC2}}{g_{o,CC2} + g_{o,CC4} + g_{in3}} = \frac{2g_{m17}}{\left(g_{o17}g_{o19}/g_{m19}\right) + \left(g_{o23}g_{o21}/g_{m21}\right) + g_{in3}}$$

A_{vd} continued on next foil

Left to right through the design problem circuit:

3. Second gain stage: completing the gain derivation

A_{vd} cont.:

$$A_{vd} = \frac{2\dfrac{2I_D}{\left(V_{GS17}-V_{Tp}\right)}}{\dfrac{I_D}{V_{A17}}\cdot\dfrac{I_D}{V_{A19}}\cdot\dfrac{\left(V_{GS19}-V_{Tp}\right)}{2I_D}+\dfrac{I_D}{V_{A23}}\cdot\dfrac{I_D}{V_{A21}}\cdot\dfrac{\left(V_{GS21}-V_{Tn}\right)}{2I_D}+g_{in3}}$$

$$= \frac{2}{\left(V_{GS17}-V_{Tp}\right)}\cdot\frac{2}{\left[\dfrac{\left(V_{GS19}-V_{Tp}\right)}{2V_{A17}V_{A19}}+\dfrac{\left(V_{GS21}-V_{Tn}\right)}{2V_{A23}V_{A21}}+\dfrac{g_{in3}}{I_D}\right]}$$

$$= \frac{2}{\left(V_{GS}-V_T\right)_{\min}}\cdot\frac{2}{\left[\dfrac{\left(V_{GS}-V_T\right)_{\min}}{V_A^2}+\dfrac{2g_{in3}}{K_{17}\left(V_{GS}-V_T\right)^2_{\min}}\right]}$$

Lesson: Bias the FETs at $(V_{GS}-V_T)_{min}$. Then make g_{in3} as small as possible and K_{17} as large as you can.*

$A_{vc} = v_{out}$ with $v_{in1} = v_{in2} = v_{ic}$,:

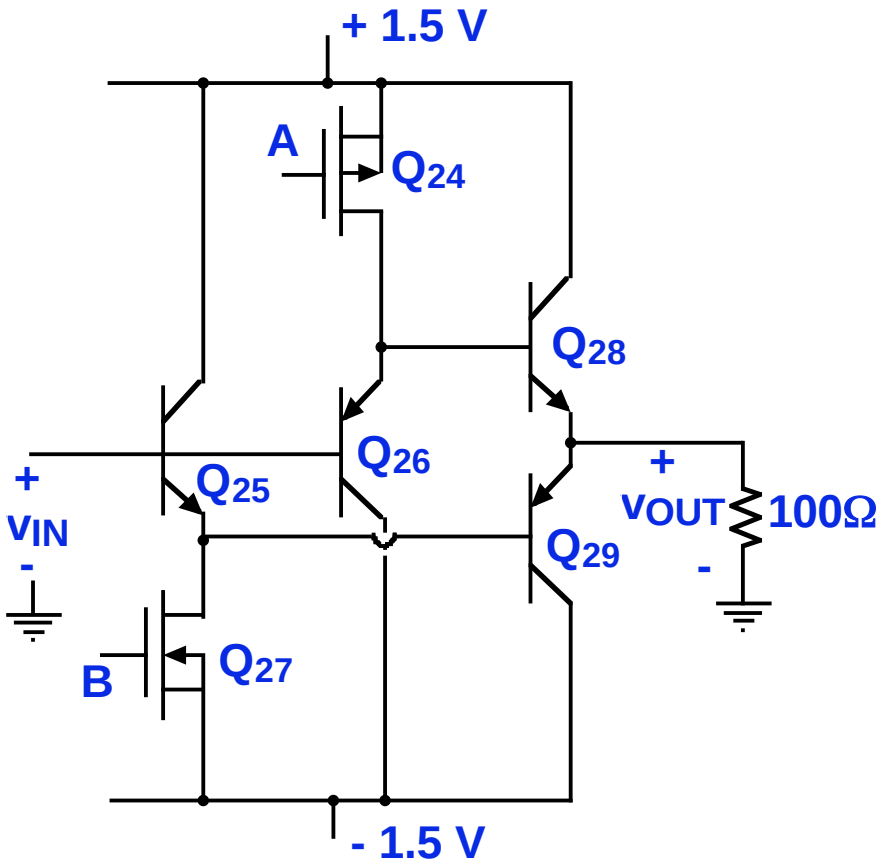
$$A_{vc} \approx \frac{1}{2}$$

Lesson: Not much can be done about A_{vc}.

* This may not be the peak gain, but it will be OK.

Left to right through the design problem circuit:

4. Third and fourth stages: emitter-followers



Comments/Observations:

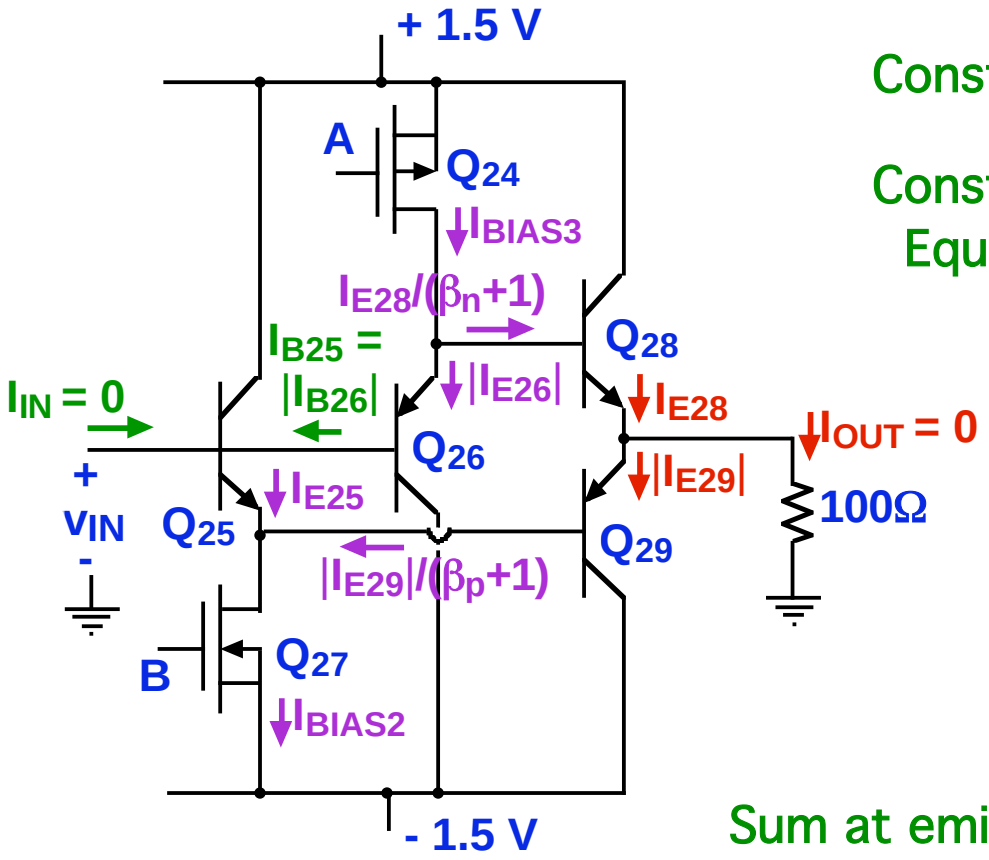
- These stages involve four emitter follower building blocks arranged as two parallel cascades of two emitter follower stages each. These stages offer the most design challenges and trade-offs of any of the stages in the design problem.
- They must be biased properly taking into account KVL and KCL constraints.
- Although they have voltage gains of almost one, they have a big effect on the overall voltage gain of the amplifier because they load the second gain stage.
- They determine the output resistance of the amplifier.

Point to ponder:

- Am I having fun yet? (This is where the fun begins.)

Left to right through the design problem circuit:

4. Third and fourth stages, cont.: biasing - getting the currents right



Constraint at output node: $I_{E28} = |I_{E29}|$

Constraint at input node: $I_{B25} = |I_{B26}|$

Equivalently: $I_{E25}/(\beta_n + 1) = |I_{E26}|/(\beta_p + 1)$

Sum at emitter of Q_{25}:

$$I_{BIAS2} = I_{E25} + |I_{E29}|/(\beta_p + 1)$$

$$= (\beta_n + 1) I_{B25} + |I_{E29}|/(\beta_p + 1)$$

$$= (\beta_n + 1)\left[I_{B25} + \frac{|I_{E29}|}{(\beta_n + 1)(\beta_p + 1)} \right]$$

Sum at emitter of Q_{26}:

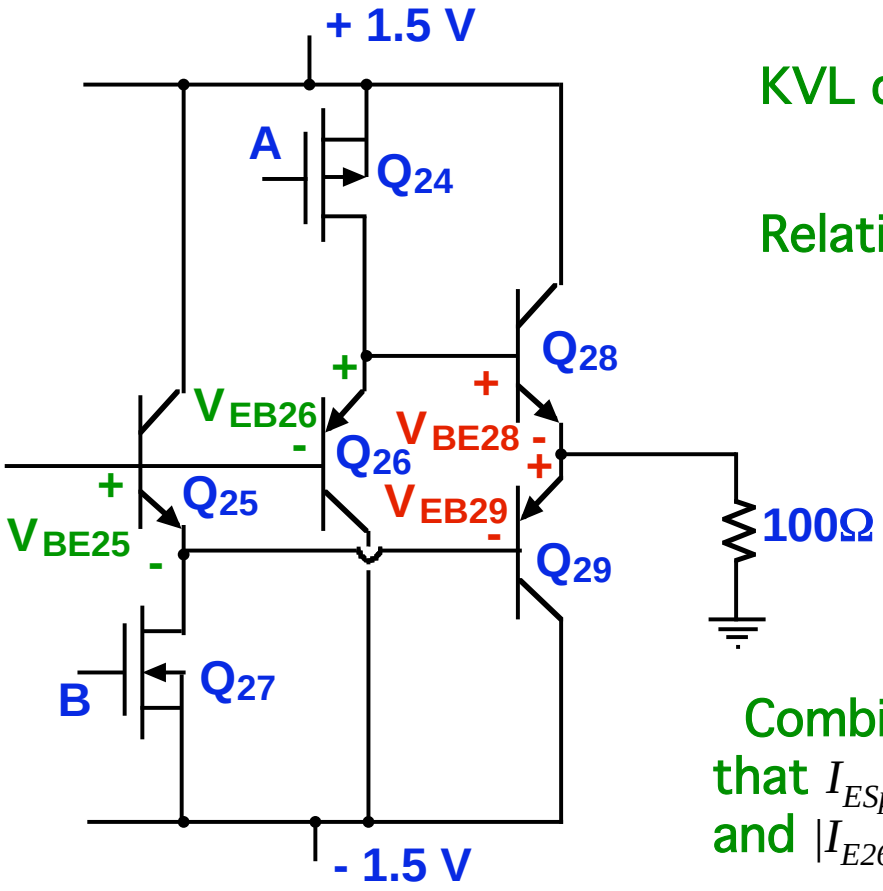
$$I_{BIAS3} = (\beta_p + 1)|I_{B26}| + I_{E28}/(\beta_n + 1) = (\beta_p + 1)\left[|I_{B26}| + \frac{I_{E28}}{(\beta_n + 1)(\beta_p + 1)} \right]$$

Combining everything: $I_{BIAS3}/I_{BIAS2} = (\beta_p + 1)/(\beta_n + 1) \approx \beta_p/\beta_n$

Lesson: The bias currents are not totally unconstrained.

Left to right through the design problem circuit:

4. Third and fourth stages, cont.: biasing - getting the voltages right



KVL constraint:

$$V_{BE28} + V_{EB29} - V_{BE25} - V_{EB26} = 0$$

Relating voltages to currents:

$$V_{BE25} = (kT/q)\ln[I_{E25}/\gamma_{25}I_{ESn}]$$

$$V_{EB26} = (kT/q)\ln[|I_{E26}|/\gamma_{26}I_{ESp}]$$

$$V_{BE28} = (kT/q)\ln[I_{E28}/\gamma_{28}I_{ESn}]$$

$$V_{BE29} = (kT/q)\ln[|I_{E29}|/\gamma_{29}I_{ESp}]$$

Combining everything, including the fact that $I_{ESp}=I_{ESn}=I_{ES}$, and the results $|I_{E28}|=I_{E29}$ and $|I_{E26}|/(\beta_p+1)=I_{E25}/(\beta_n+1)$, yields:

$$\frac{I_{E28}}{I_{E25}} = \sqrt{\frac{(\beta_p+1)}{(\beta_n+1)}\frac{\gamma_{28}\gamma_{29}}{\gamma_{25}\gamma_{26}}}$$

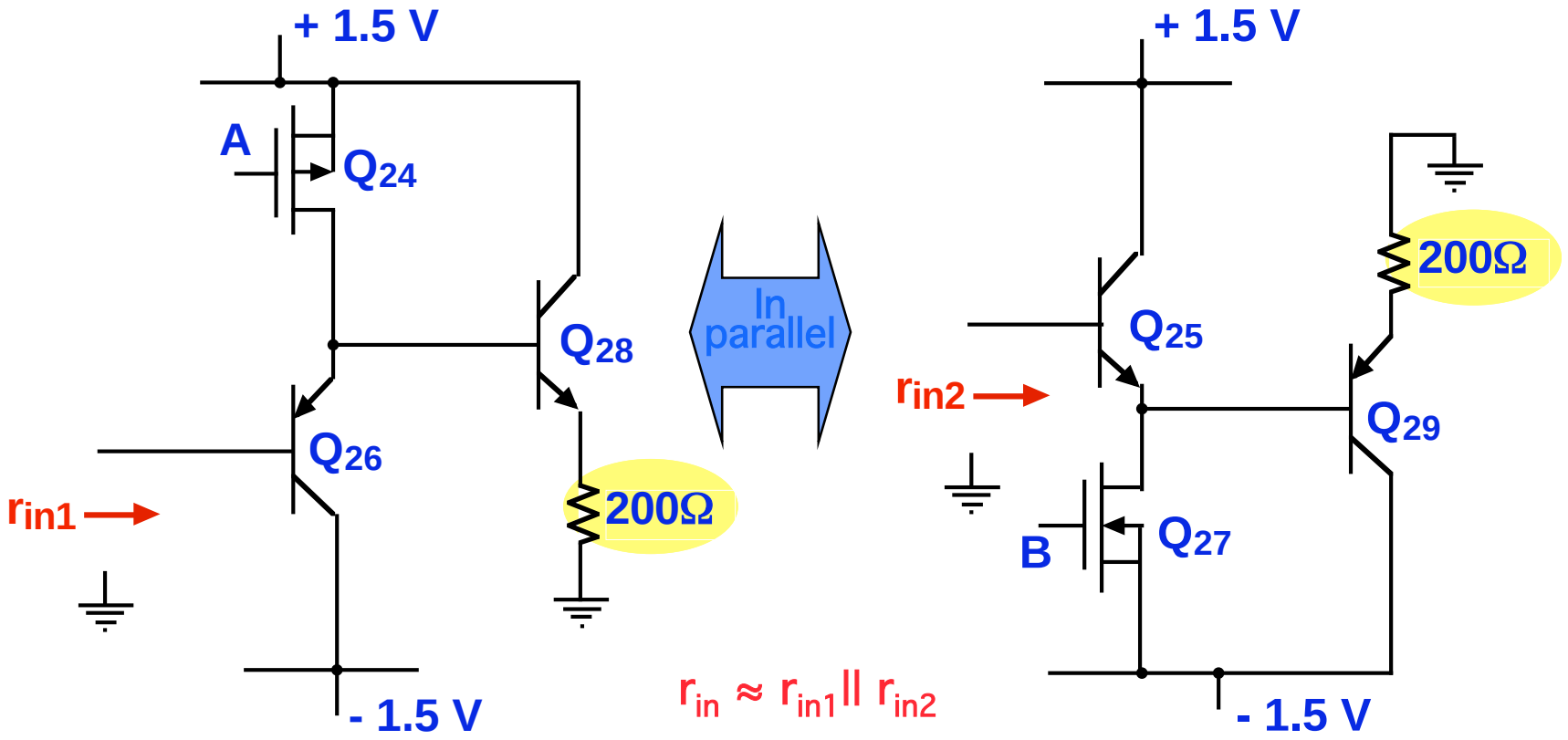
Point to ponder:

- What do the results on this foil and the last mean, and are there any other things to consider when biasing these stages?

Left to right through the design problem circuit:

4. Third and fourth stages, cont.: input resistance, r_{in}

We will use the approximation that the two emitter-follower paths can be modeled as being in parallel for purposes of calculating the input resistance.



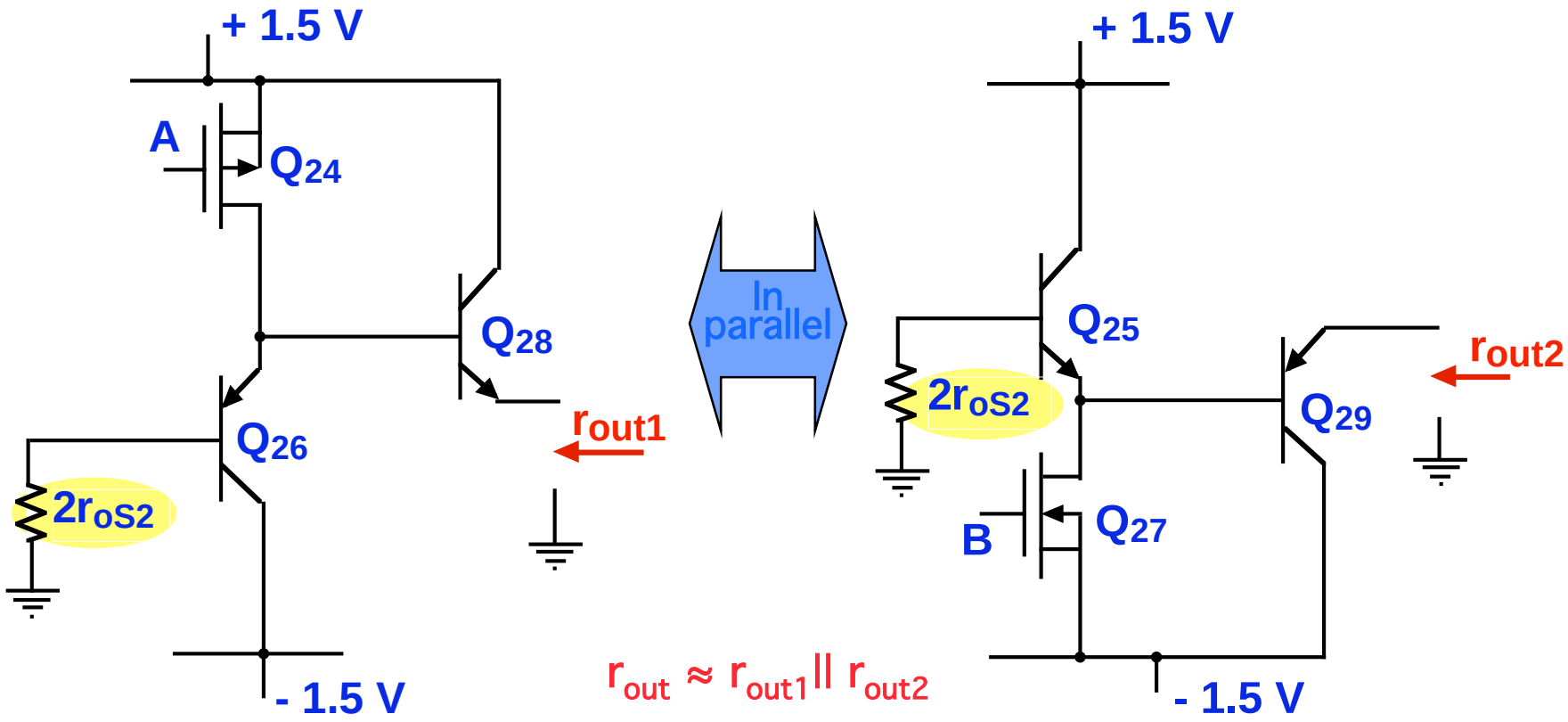
Point to ponder:

- **Remember that the ratio of I_{BIAS3} to I_{BIAS4} is constrained.**
- **Is there a penalty for picking a bias that maximizes r_{in}? What else would be impacted?**

Left to right through the design problem circuit:

4. Third and fourth stages, cont.: output resistance, r_{out}

* We will use the approximation that the two emitter-follower paths can be modeled as being in parallel for purposes of calculating the output resistance.



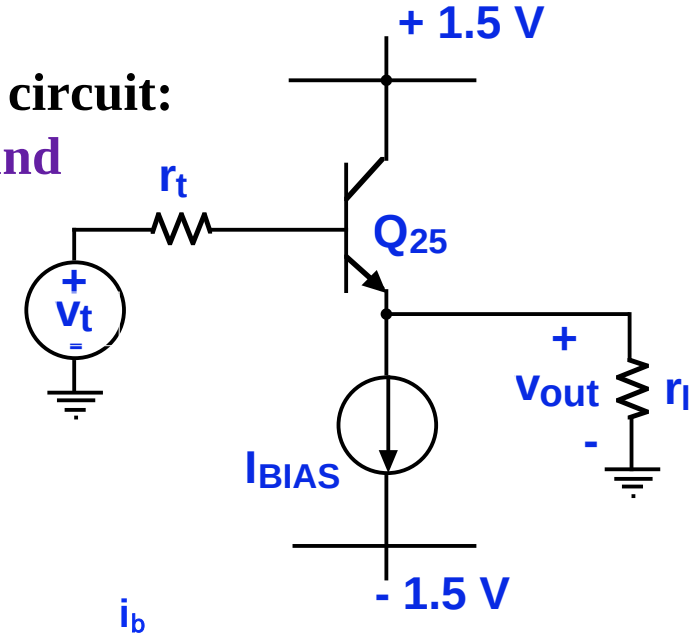
Point to ponder:

- Remember that the ratio of I_{BIAS3} to I_{BIAS4} is constrained.
- Is there a trade-off between power dissipation and r_{out}? Is there an optimum bias?

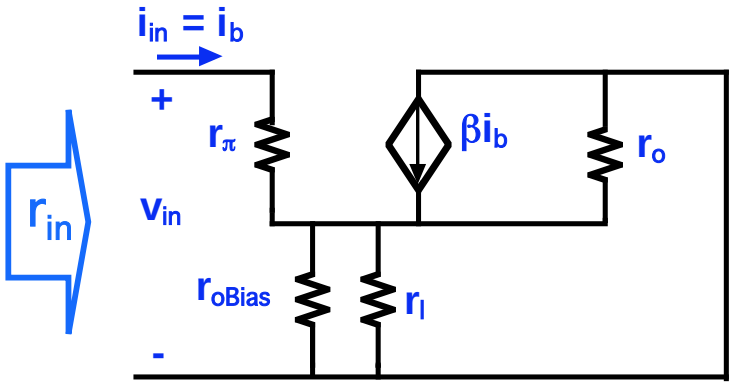
Left to right through the design problem circuit:

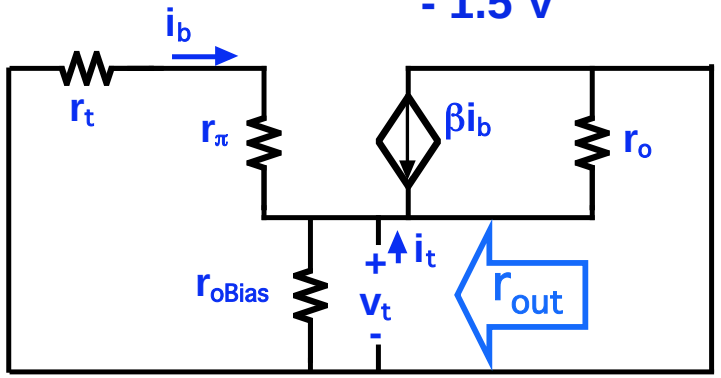
4. Third and fourth stages, cont.: r_{in} and r_{out} of an emitter follower

* Reviewing the input and output resistances of a single emitter follower stage.



Right: Emitter-follower stage
Below: LECs for finding r_{in} and r_{out}





$$r_{in} = r_\pi + (\beta+1)(r_l \parallel r_o \parallel r_{Bias}) \approx r_\pi + (\beta+1) r_l$$

$$r_{out} = 1/\left[g_o + g_{Bias} + (\beta+1)/(r_\pi + r_t)\right] \approx (r_\pi + r_t)/(\beta+1)$$

Point to ponder:

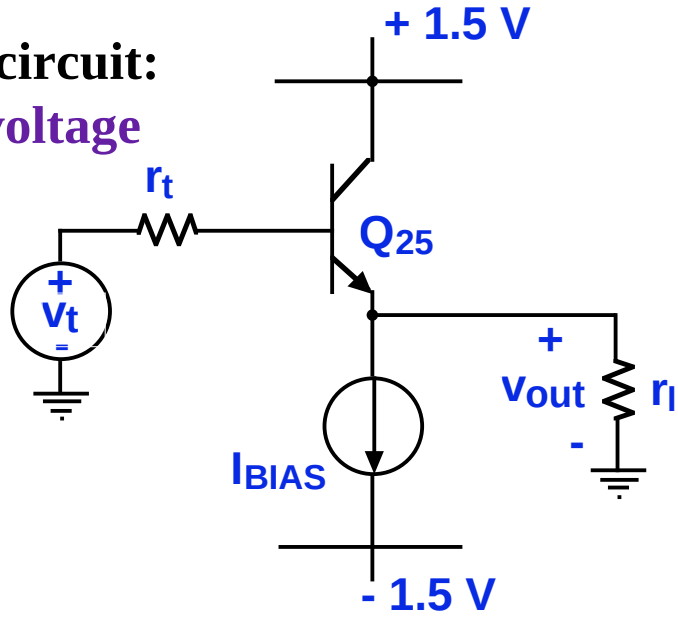
- Looking in the resistance is multiplied by (β+1); looking back it is divided by(β+1) .

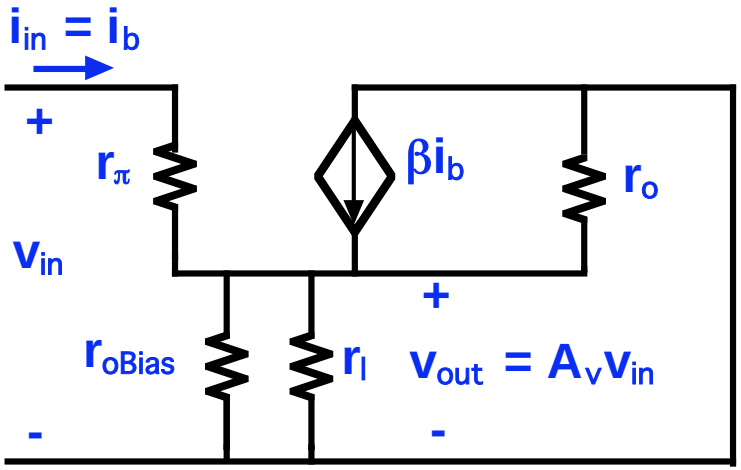
Left to right through the design problem circuit:

4. Third and fourth stages, cont.: the voltage gain, A_v, of an emitter follower

* Reviewing the voltage gain of an emitter follower stage.

Right: Emitter-follower stage
Below: LEC for finding A_v





$$v_{out} = (\beta+1) i_b (r_l \,||\, r_o \,||\, r_{Bias})$$

$$v_{in} = i_b r_\pi + (\beta+1) i_b (r_l \,||\, r_o \,||\, r_{Bias})$$

$$A_v = \frac{v_{out}}{v_{in}} = \frac{(\beta+1)(r_l \,||\, r_o \,||\, r_{Bias})}{r_\pi + (\beta+1)(r_l \,||\, r_o \,||\, r_{Bias})}$$

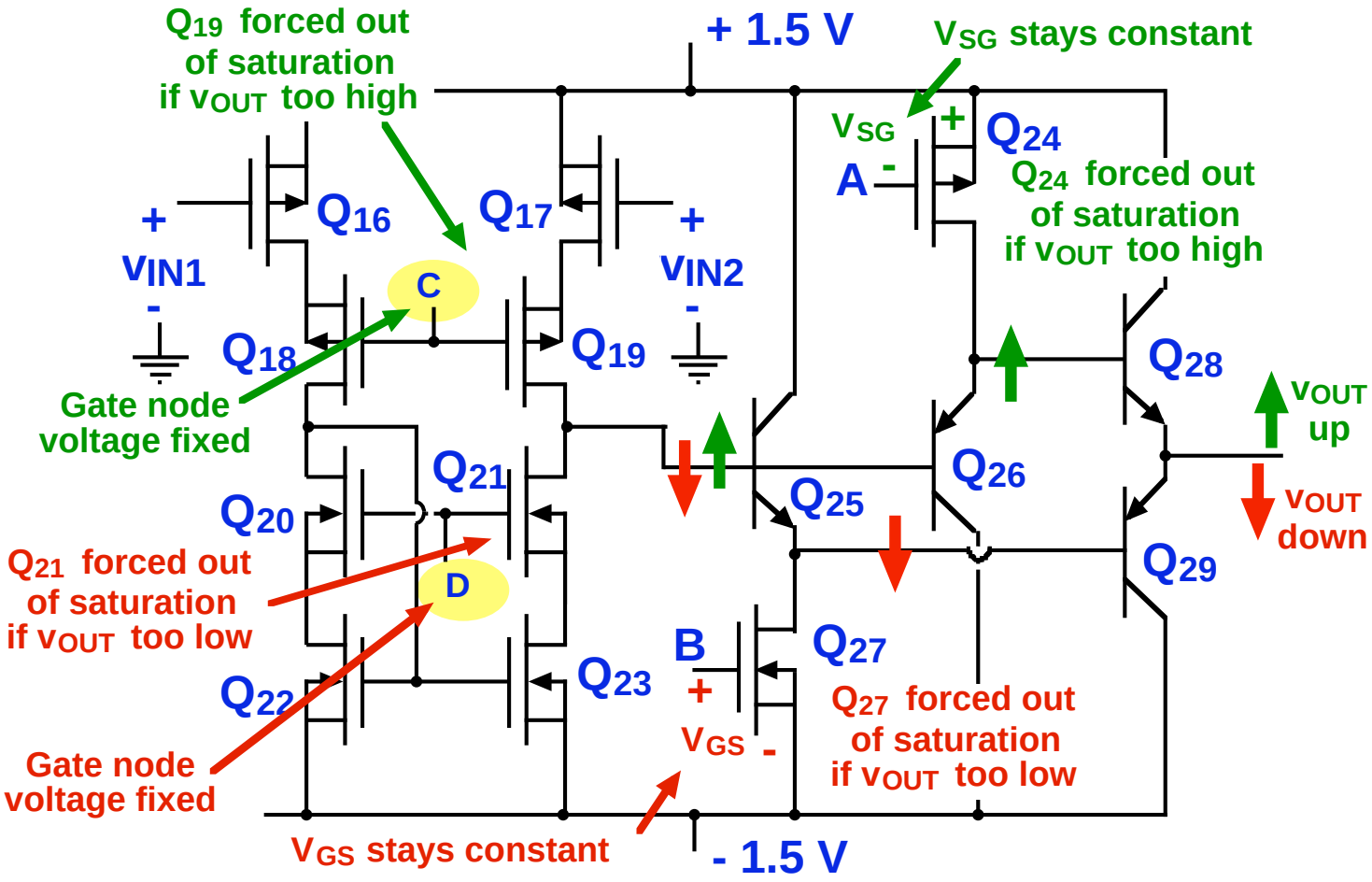
$$\approx \frac{(\beta+1) r_l}{r_\pi + (\beta+1) r_l}$$

Point to ponder:

- The voltage gains of the third-stage emitter followers (Q_{25} and Q_{26}) will likely be very close to one, but that of the stage-four followers might be noticeably less than one.

Left to right through the design problem circuit:

4. Third and fourth stages, cont.: output voltage swing

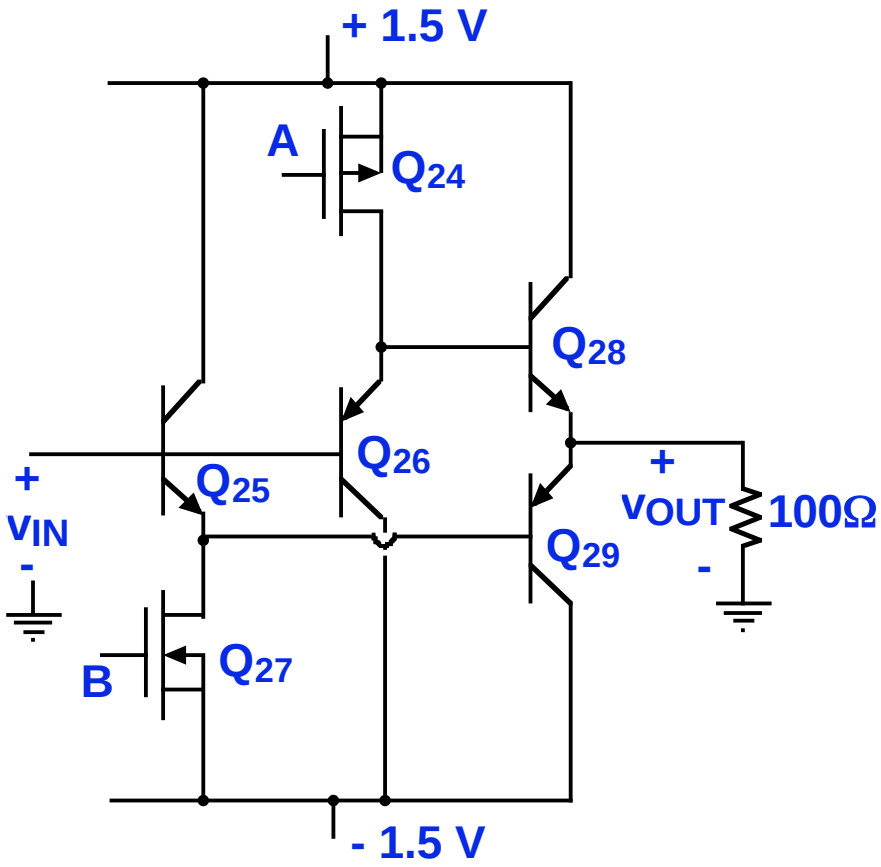


Points to ponder:

- How far + and - can the node connecting the drains of Q_{19} and Q_{21} swing?
- How low can the voltage on the drain of Q_{27} go? How high for the drain of Q_{24}?
- How much do v_{BE28} and v_{EB29} increase as $|v_{OUT}|$ inceases?

Left to right through the design problem circuit:

4. Third and fourth stages: putting it all together



Point to ponder:

- Now that I know everything, how can I meet the specs?

Comments/Observations:

- These stages involve four emitter follower building blocks arranged as two parallel cascades of two emitter follower stages each. These stages offer the most design challenges and trade-offs of any of the stages in the design problem.
- They must be biased properly taking into account KVL and KCL constraints.
- Although they have voltage gains of almost one, these stages have a big effect on the overall voltage gain of the amplifier because they load the second gain stage.
- These stages determine the output resistance of the amplifier.
- I_{BIAS3} and I_{BIAS4} set the bias levels of Q_{25} and Q_{26}. The bias levels of Q_{28} and Q_{29} are set by the γ's.
- A reasonable choice is to make $\gamma_{28} = \gamma_{29}$, and $\gamma_{25} = [(\beta_n+1)/(\beta_p+1)]\gamma_{26}$, in which case:

$$I_{E28}/I_{E25} = \gamma_{28}/\gamma_{25}$$

Left to right through the design problem circuit:

6. Overall gain expression

The defining relationships:

$$v_{out} = A_{vd} v_{id} + A_{vc} v_{ic} = A_{vd} \left(v_{in1} - v_{in2} \right) + A_{vc} \left(v_{in1} + v_{in2} \right) / 2$$

The difference-mode gain:

$$A_{vd} = A_{vd1} \cdot A_{vd2} \cdot A_{v3} \cdot A_{v4}$$

$$= \frac{-g_{m13}}{2\left(g_{013} + 2g_{o9}\right)} \cdot \frac{-2g_{m17}}{\left(\frac{g_{017}g_{019}}{g_{m19}}\right) + \left(\frac{g_{023}g_{021}}{g_{m23}}\right) + g_{in3}} \cdot 1 \cdot \frac{\left(\beta_n + 1\right) 2r_l}{r_{\pi 28} + \left(\beta_n + 1\right) 2r_l}$$

$$r_l = 100\,\Omega$$

The common-mode gain:

$$A_{vc} = A_{vc1} \cdot A_{vc2} \cdot A_{v3} \cdot A_{v4} = \frac{-g_{015}}{4g_{m9}} \cdot \frac{-1}{2} \cdot 1 \cdot \frac{\left(\beta_n + 1\right) 2r_l}{r_{\pi 28} + \left(\beta_n + 1\right) 2r_l}$$

Point to ponder:

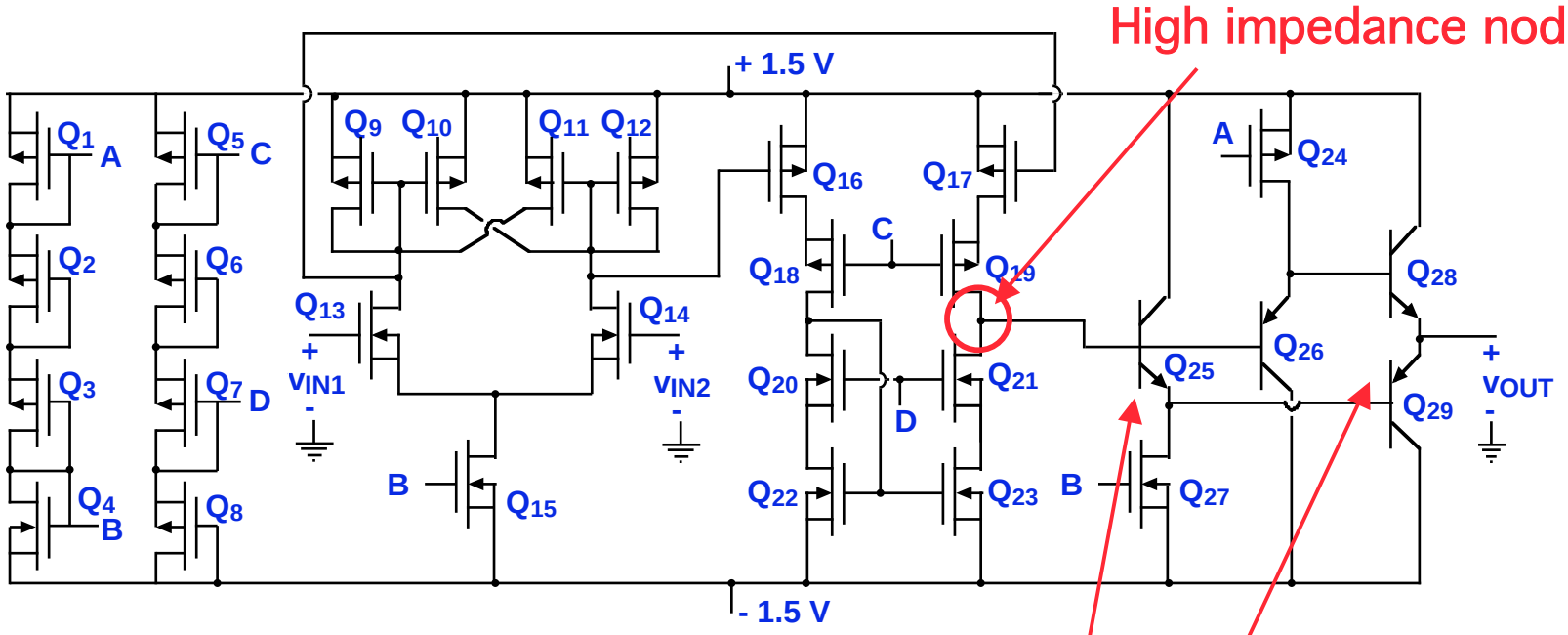
- **The follower stages treat the difference and common mode outputs the same.**
- **Let's put it all together and see what your design can do!**

Left to right through the design problem circuit:

5. DC offset of a differential amplifier (OP-amp)

Procedure for finding the DC offset:

I. Identify the high impedance node* in the amplifier, and calculate what the voltage on that node is when the output voltage is zero.



Node voltage when $v_{OUT} = 0$: $V_{NODE\text{-}I} = V_{BE25} - V_{EB29} \approx 0$ V

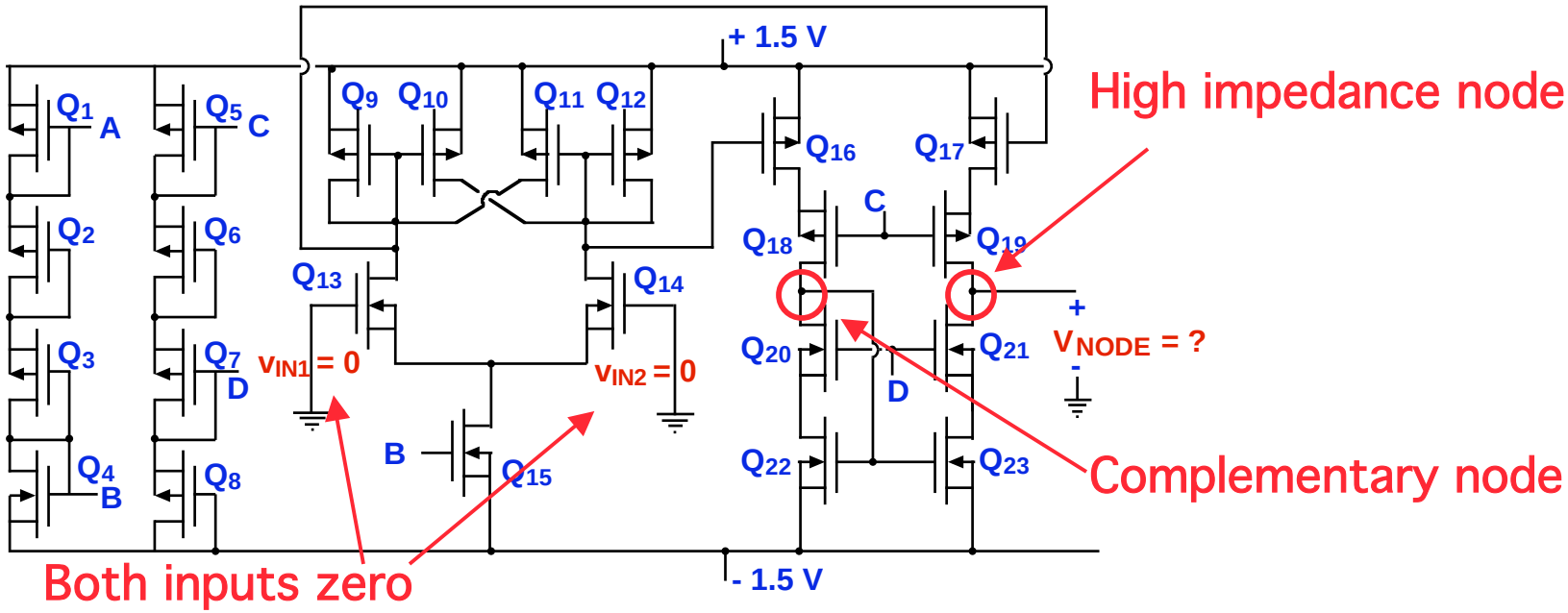
* Example: The output node of a CMOS inverter is an high impedance node. When both MOSFETs were saturated the voltage on this node could take on a range of values, and we couldn't say what v_{OUT} was when v_{IN} was $V_{DD}/2$.

Left to right through the design problem circuit:

5. DC offset of a differential amplifier (OP-amp)

Procedure for finding the DC offset:

II. Disconnect the circuit following the high impedance node and calculate the voltage on the node when $v_{IN1} = v_{IN2} = 0$, assuming perfect symmetry and matching. Call this voltage $V_{NODE-II}$.



With perfect matching and symmetry,the voltage on the high impedance node will equal that on the complementary node. In this case $V_{NODE-II} = -1.5V + V_{GS22}$

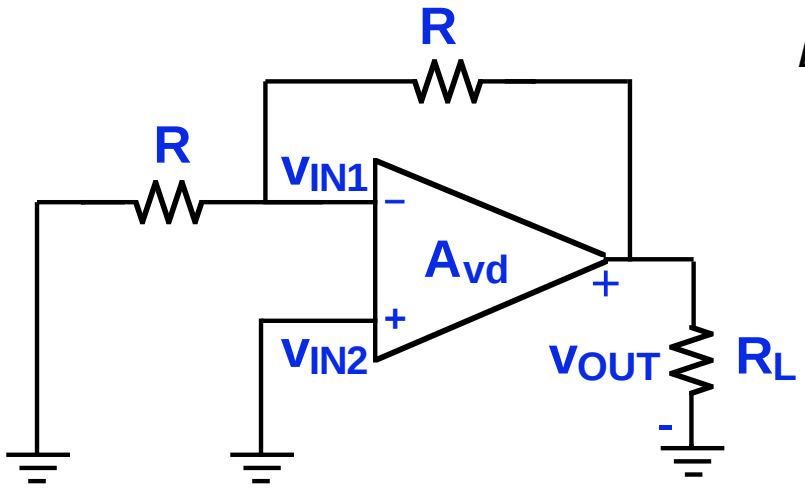
Left to right through the design problem circuit:

5. DC offset of a differential amplifier (OP-Amp)

Procedure for finding the DC offset:

III. Knowing the differential voltage gain of the stage, Avd, we can calculate the DC off-set at the output by subtracting the voltage calculated in Step I, which we can call V_{NODE-I}, from the voltage calculated in Step II, $V_{NODE-II}$.

When $v_{IN1} - v_{IN2} = (V_{NODE-I} - V_{NODE-II})/A_{vd}$, V_{OUT} is on the same order and thus essentially zero. We will define this value of $v_{IN1} - v_{IN2}$ to be the DC offset, certainly compared to $(V_{NODE-I} - V_{NODE-II})$.



$$DC\ offset = (V_{NODE-I} - V_{NODE-II})/A_{vd}$$

Example: In the design problem, if A_{vd} turns out to be -1×10^4, and $(V_{NODE-I} - V_{NODE-II})$ is -0.9V, then the DC offset is 90 μV.

6.012 Microelectronic Devices and Circuits

Fall 2009