# Lecture 21 - Multistage Amplifiers (I)

## Multistage Amplifiers

November 22, 2005

**Contents**:



## Reading assignment:

Howe and Sodini, Ch. 9, §§9.1-9.3

# Key questions

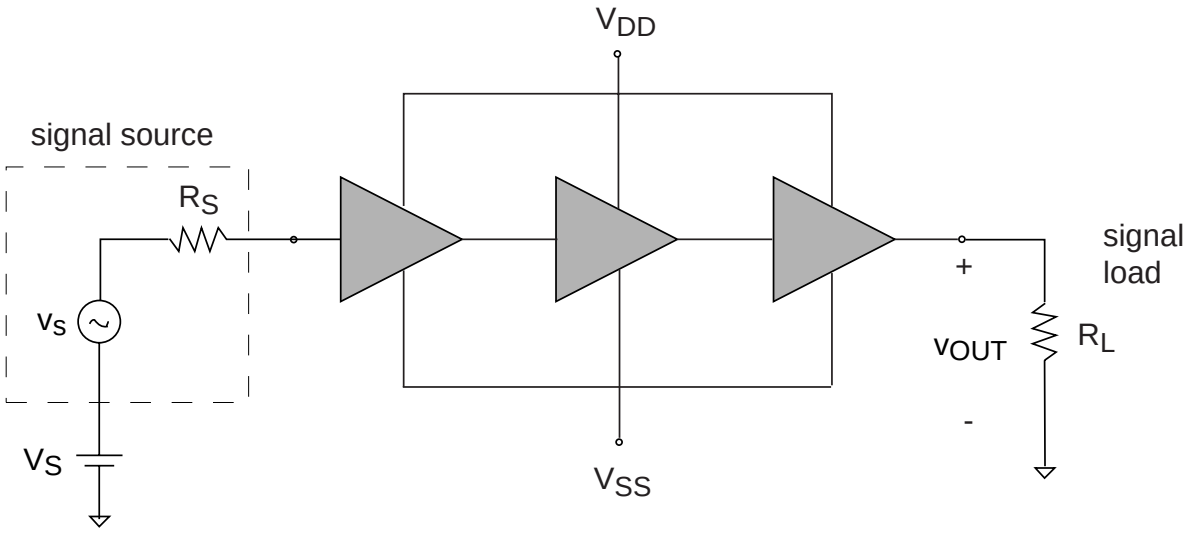
- How can one build a wide range of high-performance amplifiers using the single-transistor stages studied so far?
- What are the most important considerations when assembling mulstistage amplifiers:
  - regarding interstage loading?
  - regarding interstage biasing?

# 1. Introduction

Amplifier requirements are often demanding:

- must adapt to specific kinds of signal source and load,
- must deliver sufficient gain

Single-transistor amplifier stages are very limited in what they can accomplish ⇒ *multistage amplifier*.




Issues:

- What amplifying stages should be used and in what order?
- What devices should be used, BJT or MOSFET?
- How is biasing to be done?

## □ Summary of single stage characteristics:

| **stage** | $A_{vo},\ G_{mo},\ A_{io}$ | $R_{in}$ | $R_{out}$ | **key function** |
|---|---|---|---|---|
| CS | $G_{mo} = g_m$ | $\infty$ | $r_o//r_{oc}$ | transcond. amp. |
| CD | $A_{vo} \simeq \frac{g_m}{g_m+g_{mb}}$ | $\infty$ | $\frac{1}{g_m+g_{mb}}$ | voltage buffer |
| CG | $A_{io} \simeq -1$ | $\frac{1}{g_m+g_{mb}}$ | $r_{oc}//[r_o(1+g_mR_S)]$ | current buffer |
| CE | $G_{mo} \simeq g_m$ | $r_\pi$ | $r_o//r_{oc}$ | transcond. amp. |
| CC | $A_{vo} \simeq 1$ | $r_\pi + \beta(r_o//r_{oc}//R_L)$ | $\frac{1}{g_m} + \frac{R_S}{\beta}$ | voltage buffer |
| CB | $A_{io} \simeq -1$ | $\frac{1}{g_m}$ | $r_{oc}//\{r_o[1+g_m(r_\pi//R_S)]\}$ | current buffer |

## □ Key differences between BJT's and MOSFETs:

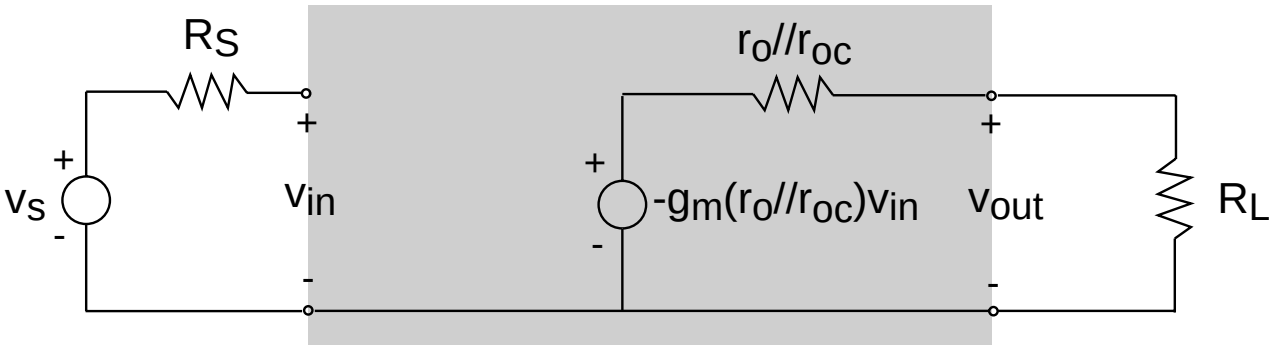
| **BJT** | | **MOSFET** |
|---|---|---|
| $I_B = \frac{I_C}{\beta}$ | $\gg$ | $I_G = 0$ |
| $g_m = \frac{qI_C}{kT}$ | $>$ | $g_m = \sqrt{2\frac{W}{L}\mu C_{ox} I_D}$ |
| $r_o = \frac{V_A}{I_C}$ | $>$ | $r_o = \frac{1}{\lambda I_D}$ |

# 2. CMOS multistage voltage amplifier

☐ Goals:

- high voltage gain
- high $R_{in}$
- low $R_{out}$

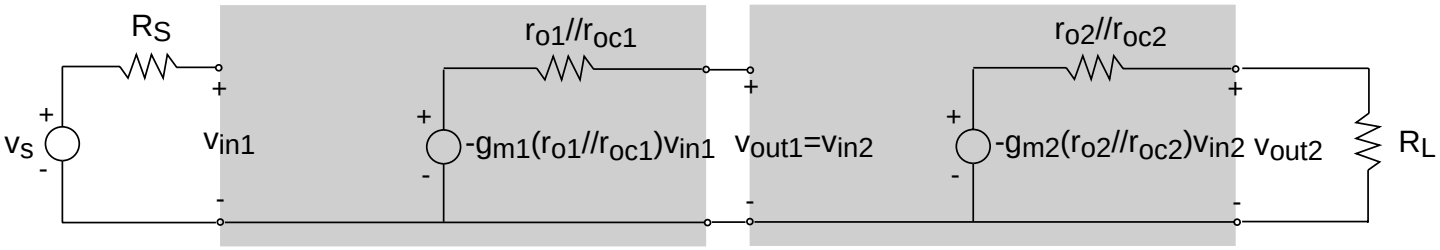
☐ Good starting point: CS stage




✓ • $R_{in} = \infty$ excellent!

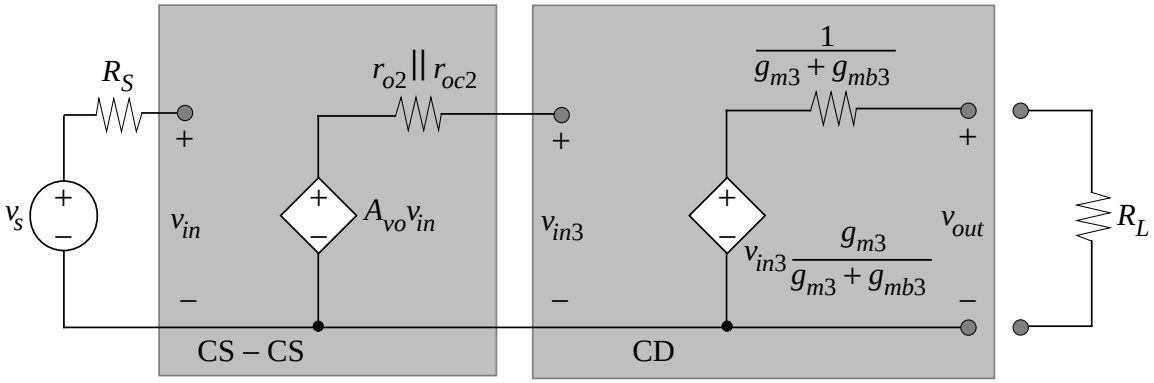
- $A_{vo} = -g_m(r_o//r_{oc})$, probably insufficient
- $R_{out} = r_o//r_{oc}$, too high

## ☐ Add second CS stage to get more gain:




- ✓ $R_{in} = \infty$
- ✓ $A_{vo} = g_{m1}(r_{o1}//r_{oc1})g_{m2}(r_{o2}//r_{oc2})$
- but $R_{out} = r_{o2}//r_{oc2}$, still high

## ☐ Add CD stage at output:



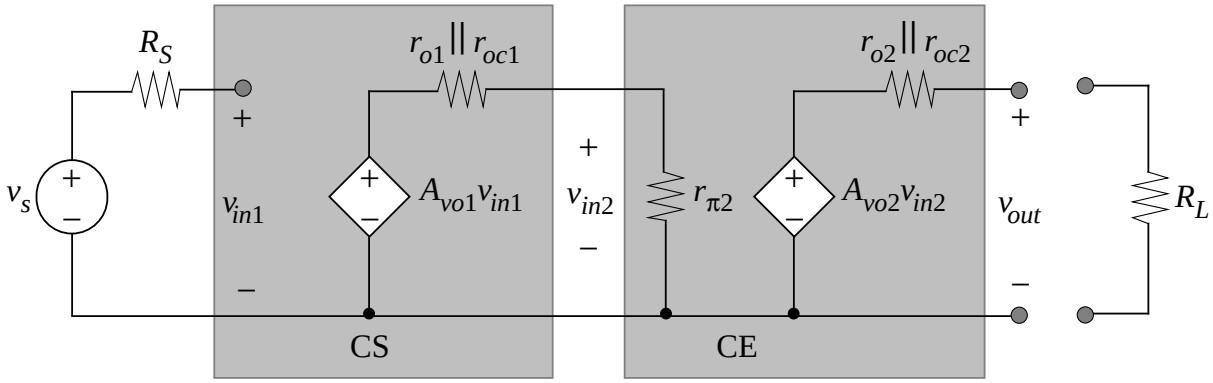

- ✓ $R_{in} = \infty$
- ✓ $A_{vo} = g_{m1}(r_{o1}//r_{oc1})g_{m2}(r_{o2}//r_{oc2})\frac{g_{m3}}{g_{m3}+g_{mb3}}$, still high
- ✓ $R_{out} = \frac{1}{g_{m3}+g_{mb3}}$, now small

## 3. BiCMOS multistage voltage amplifier

□ $A_{vo}(CE) > A_{vo}(CS)$ because $r_o(BJT) > r_o(MOSFET)$ and $g_m(BJT) > g_m(MOSFET)$ but...

CS stage is best first stage, since $R_{in} = \infty$.

□ Add CE stage following CS stage?




Trouble is interstage loading degrades gain:

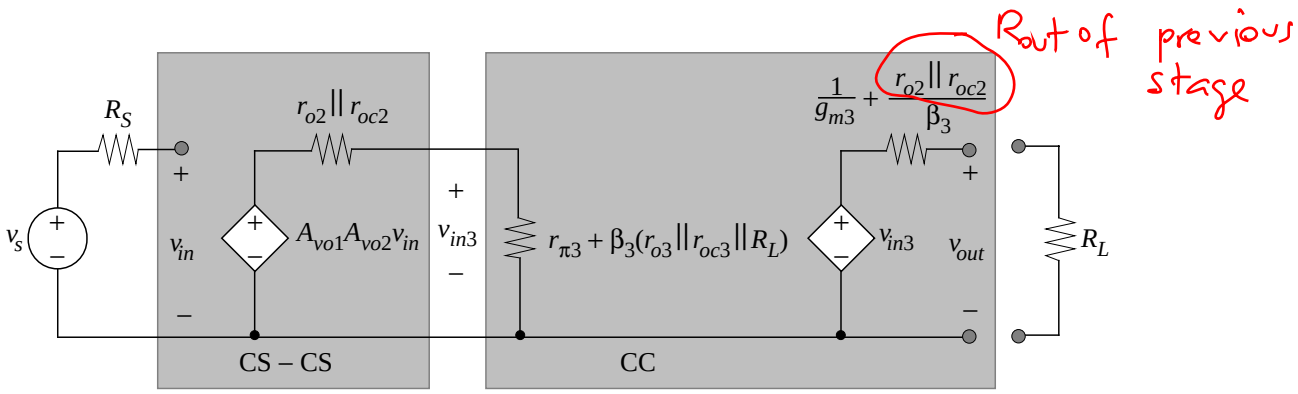
$$R_{out1} = r_{o1}//r_{oc1} \gg R_{in2} = r_{\pi 2}$$

Voltage divider between stages:

$$\frac{R_{in2}}{R_{out1} + R_{in2}} = \frac{r_{\pi 2}}{r_{o1}//r_{oc1} + r_{\pi 2}} \simeq \frac{r_{\pi 2}}{r_{o1}//r_{oc1}} \ll 1$$

Additional gain provided by CE stage more than lost in interstage loading.

□ Use two CS stages, but add CC stage at output:




Interstage loading:

$$R_{out2} = r_{o2}//r_{oc2}, \quad R_{in3} = r_{\pi 3} + \beta_3(r_{o3}//r_{oc3}//R_L)$$

Then, interstage loss:

$$\frac{R_{in3}}{R_{out2} + R_{in3}} = \frac{r_{\pi 3} + \beta_3(r_{o3}//r_{oc3}//R_L)}{r_{o2}//r_{oc2} + r_{\pi 3} + \beta_3(r_{o3}//r_{oc3}//R_L)}$$

better than trying to use a CE stage, but still pretty bad.

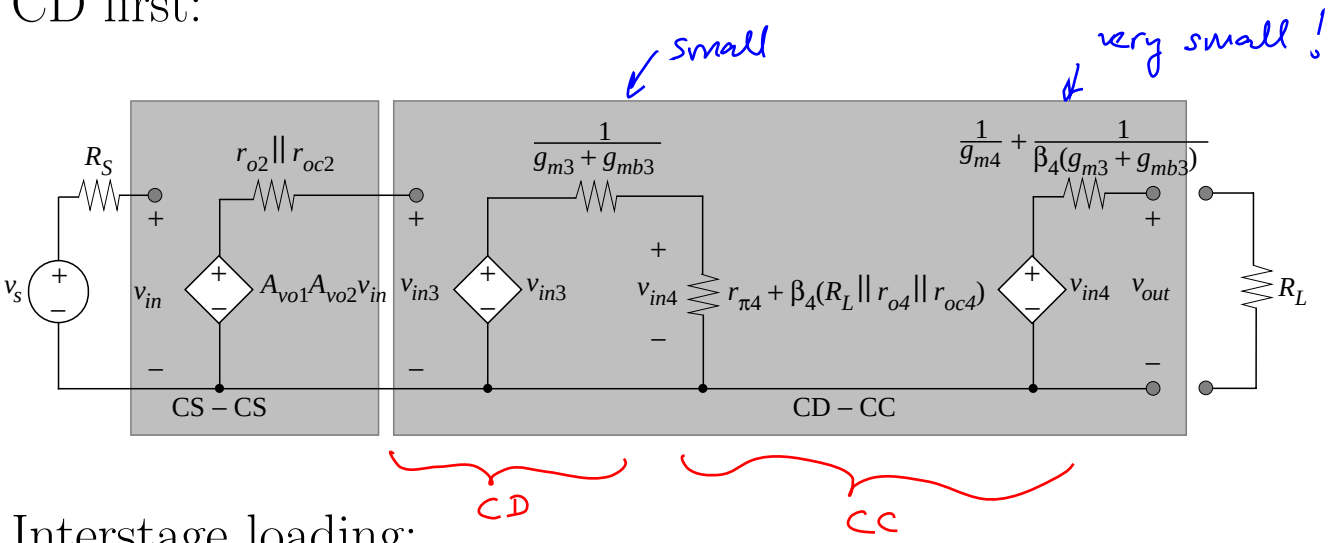
Benefit is that $R_{out}$ has improved:

$$R_{out} = R_{out3} = \frac{1}{g_{m3}} + \frac{R_{out2}}{\beta_3} = \frac{1}{g_{m3}} + \frac{r_{o2}//r_{oc2}}{\beta_3}$$

Since, in general, $g_m(BJT) > g_m(MOSFET)$, $R_{out}$ could be better than CD output stage if $r_{o2}//r_{oc2}$ is not too large. Otherwise, CD stage output is better.

□ Better voltage buffer: cascade CC and CD output stages.

What is best order? Since $R_{in}(CD) = \infty$, best to place CD first:




Interstage loading:

$$\frac{R_{in3}}{R_{out2} + R_{in3}} = 1$$

$$\frac{R_{in4}}{R_{out3} + R_{in4}} = \frac{r_{\pi 4} + \beta_4(r_{o4}//r_{oc4}//R_L)}{\frac{1}{g_{m3}+g_{mb3}} + r_{\pi 4} + \beta_4(r_{o4}//r_{oc4}//R_L)} \simeq 1$$

and excellent output resistance:

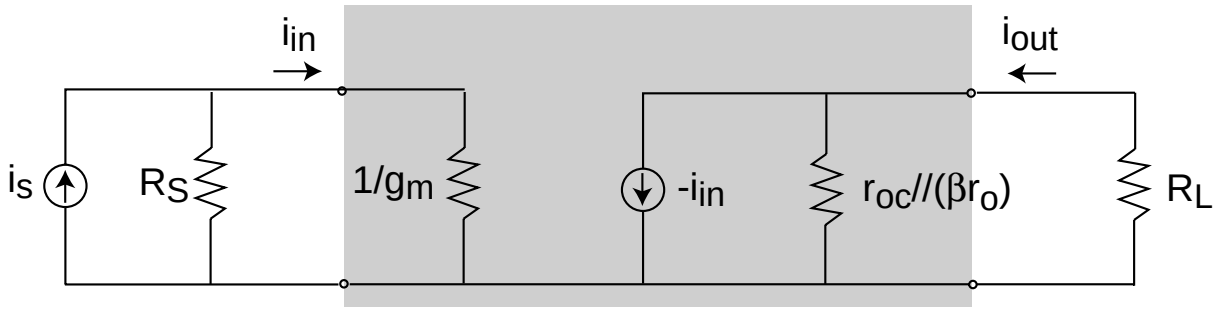
$$R_{out} = R_{out4} = \frac{1}{g_{m4}} + \frac{R_{out3}}{\beta_4} = \frac{1}{g_{m4}} + \frac{1}{\beta_4(g_{m3} + g_{mb3})}$$

# 4. BiCMOS current buffer

□ Goals:

- Unity current gain
- very low $R_{in}$
- very high $R_{out}$

Start with common-base stage:




✓ • $A_{io} = -1$

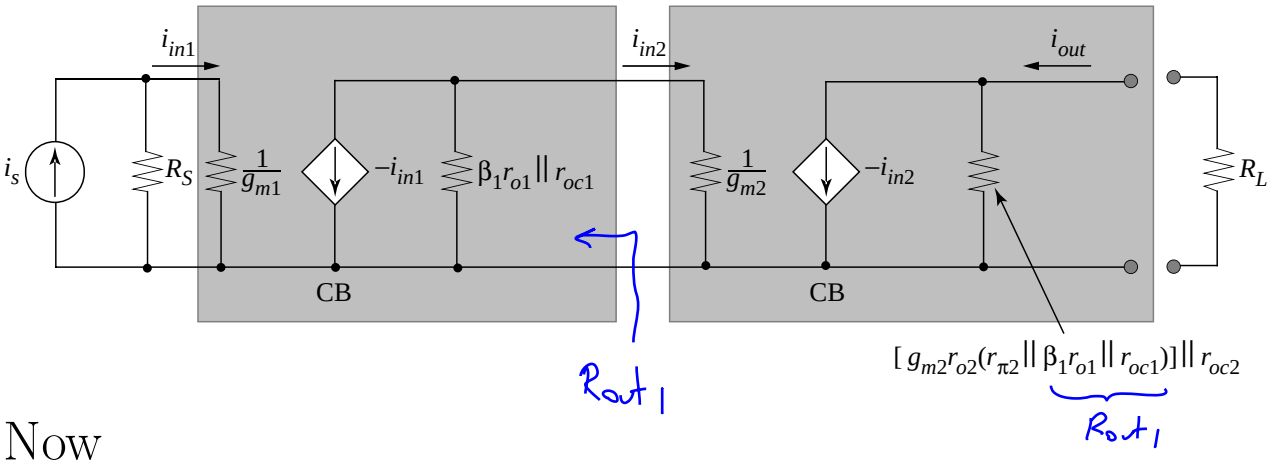
✓ • $R_{in} = \frac{1}{g_m}$

• $R_{out} = r_{oc}//\{r_o[1 + g_m(r_\pi//R_S)]\}$

Note that if $R_S$ is not too low, $R_{out} \simeq r_{oc}//(\beta r_o)$.

Can we further increase $R_{out}$ by adding a second CB stage?

□ CB-CB current buffer:




Now

$$R_{out} = R_{out2} = r_{oc2}//\{r_{o2}[1 + g_{m2}(r_{\pi 2}//R_{out1})]\}$$

Plugging in $R_{out1} \simeq r_{oc1}//(\beta_1 r_{o1})$,

$$R_{out} = r_{oc2}//\{r_{o2}[1 + g_{m2}(r_{\pi 2}//r_{oc1}//\beta_1 r_{o1})]\}$$

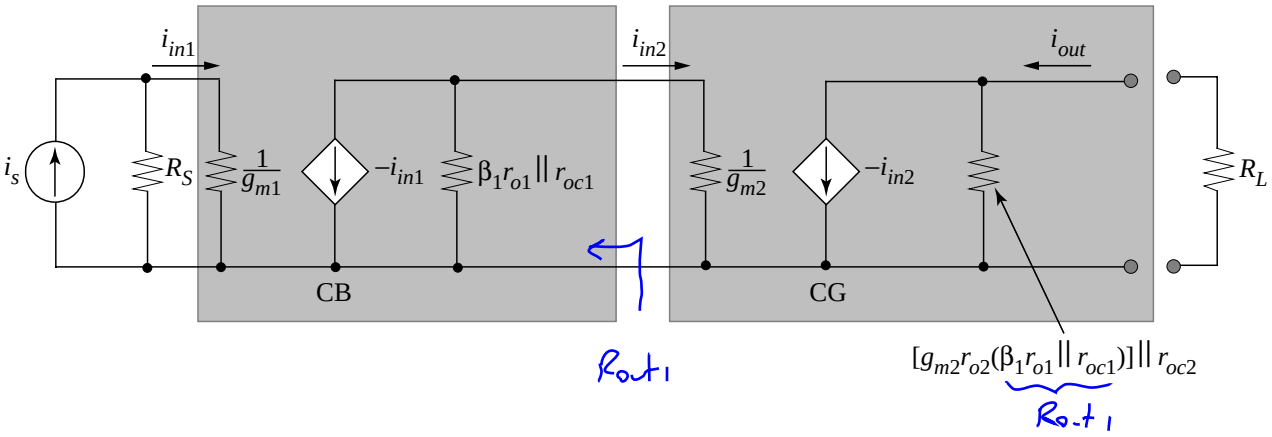
But, since $r_{\pi 2} \ll r_{oc1}//(\beta_1 r_{o1})$, then

$$R_{out} \simeq r_{oc2}//[r_{o2}(1 + g_{m2} r_{\pi 2})] \simeq r_{oc2}//(\beta_2 r_{o2})$$

Did not improve anything! The base current limits the number of CB stages that improve $R_{out}$ to just one.

Since CG stage has no gate current, cascade it behind CB stage.

□ CB-CG current buffer:




$$R_{out} = R_{out2} = r_{oc2} // [r_{o2}(1 + g_{m2} R_{out1})]$$

with $R_{out1} \simeq r_{oc1} // (\beta_1 r_{o1})$,

$R_{out}$ of CB

$$R_{out} = r_{oc2} // [r_{o2} g_{m2} (r_{oc1} // \beta_1 r_{o1})]$$

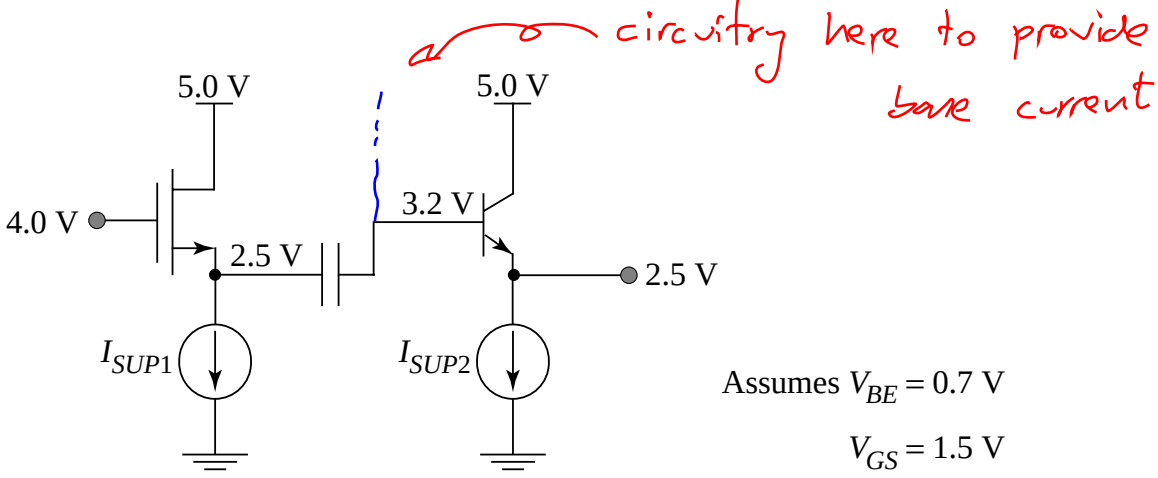
✓ Now $R_{out}$ has improved by about $g_{m2} r_{o2}$, but only to the extent that $r_{oc2}$ is high enough...

# 5. Coupling amplifier stages

## ☐ Capacitive coupling

Capacitors of large enough value behave as AC short, so signal goes through but bias is independent for each stage.

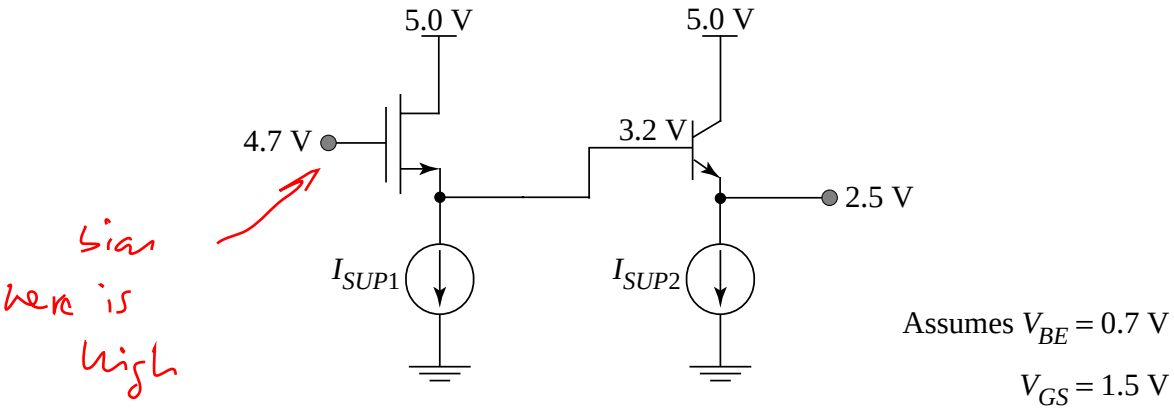
Example, CD-CC voltage buffer:




- Advantages:
  - can select bias point for optimum operation
  - can select bias point close to middle of rails for maximum signal swing
- Disadvantages:
  - to approximate AC short, need large capacitors that consume significant area

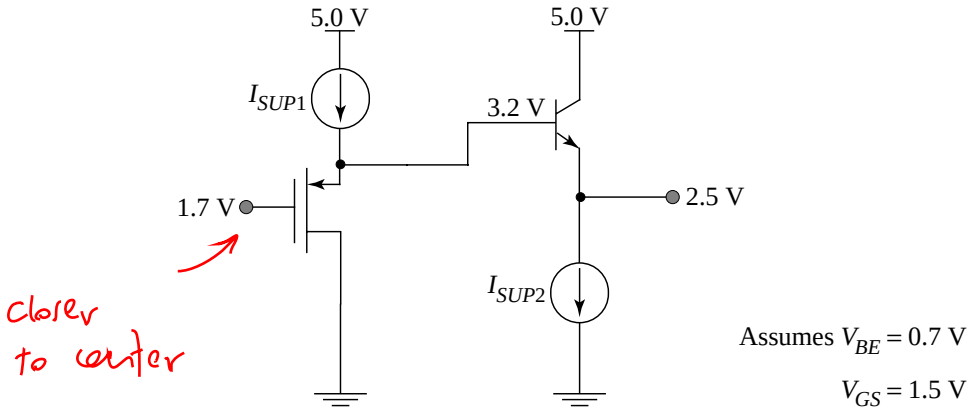
□ DIRECT COUPLING: share bias points across stages.

Example, CD-CC voltage buffer:




- Advantages:
  - no capacitors: compact
- Disadvantages:
  - bias point shared: constrains design
  - bias shifts from stage to stage and can stray too far from center of range

Solution: use PMOS CD stage:



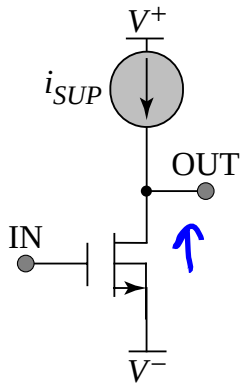
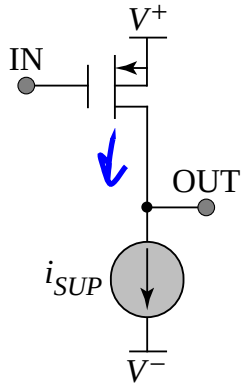
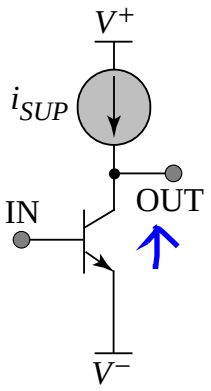
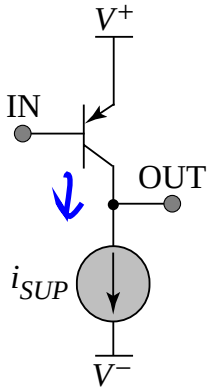
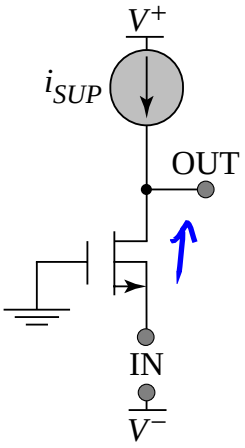
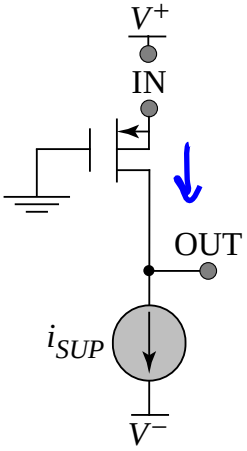
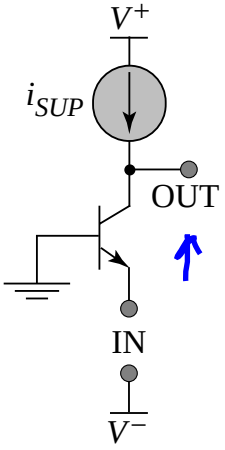
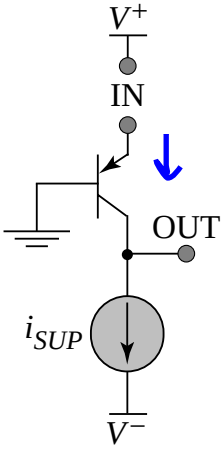
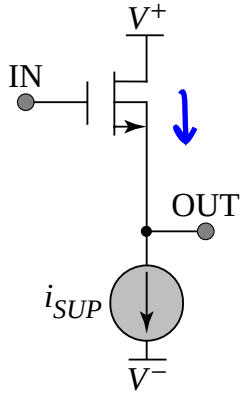
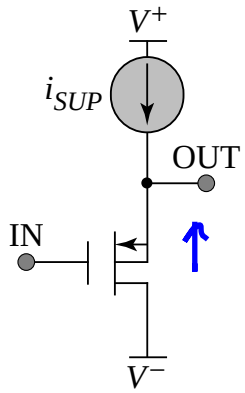
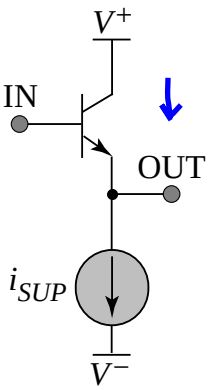
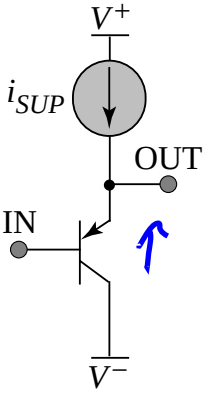

Trade-off: $g_m$(PMOS)< $g_m$(NMOS) $\rightarrow$ higher $R_{out}$

In BiCMOS voltage amplifier:

$$R_{out} = \frac{1}{g_{m4}} + \frac{1}{\beta_4(g_{m3} + g_{mb3})}$$

smaller using PMOS

# □ Summary of DC shifts through amplifier stages:

| **Amplifier Type** | **Transistor Type** | | | |
|---|---|---|---|---|
| | NMOS | PMOS | npn | pnp |
| Common Source/ Common Emitter (*CS*/*CE*) |  |  |  |  |
| Common Gate/ Common Base (*CG*/*CB*) |  |  |  |  |
| Common Drain/ Common Collector (*CD*/*CC*) |  |  |  |  |

Important difference in bias shift between stages in BJT and MOSFET amps:

- In BJT (for npn):

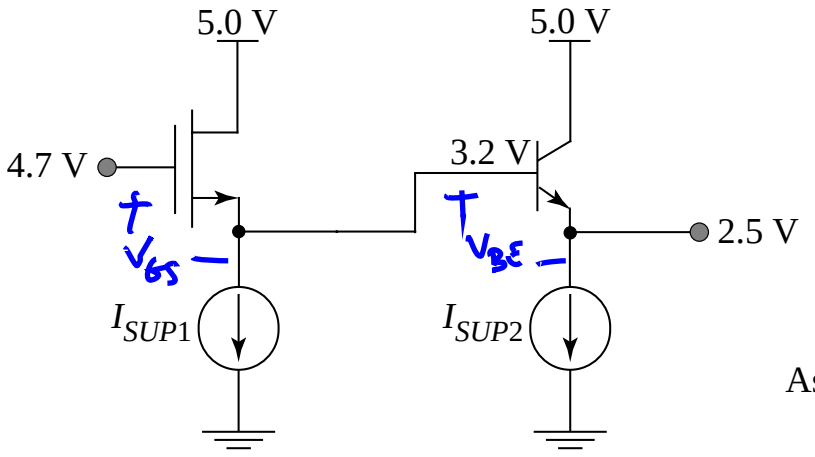
$$V_{BE} \simeq V_{BE,on}$$

rather independent of transistor size and current level.

- In MOSFET (for nMOSFET):

$$V_{GS} = V_T + \sqrt{\frac{2I_D}{\mu_n C_{ox}} \frac{L}{W}}$$

Can be engineered through bias current and transistor geometry.




Assumes $V_{BE} = 0.7$ V

$V_{GS} = 1.5$ V

# Key conclusions

- To achieve amplifier design goals, several stages often needed.
- In multistage amplifiers, different stages used to accomplish different goals:
  - voltage gain: common-source, common emitter
  - voltage buffer: common-drain, common collector
  - current buffer: common-gate, common base
- In multistage amplifiers must pay attention to interstage loading to avoid unnecessary losses.
- In *direct-coupled* amplifiers, bias is shared between adjoining stages:
  - must select compromise bias,
  - must pay attention to bias shift from stage to stage.