

PROFESSOR In this problem, we are going to take a look at the timing constraints associated with sequential logic circuits. We are given a generic state machine diagram, which has two state bits. We are also given the timing parameters for the combinational logic and the state register. Using this data we want to determine the largest value for the register's whole time that allows the necessary timing specifications to be met.

In order to satisfy the whole time of the register, the input to the register must remain stable until t_{HOLD} after the clock edge. The fastest that a new change can propagate to the input of the register is found by taking the sum of the contamination delays along the shortest path to that input. That is $[? t_{\text{CD}} ?]$ of the register plus t_{CD} of the logic. So t_{HOLD} must be less than or equal to t_{CD} of the register plus t_{CD} of the logic.

Plugging in the given contamination delays, we find that t_{HOLD} must be less than or equal to 0.1 plus 0.2, which equals 0.3 nanoseconds. What is the smallest value for the period of the clock that will meet the timing specifications? The clock period must be long enough for the data to pass through the entire circuit and be ready and stable for t_{SETUP} before the next period begins.

The data in this circuit must propagate through the register and the combinational logic. So the constraint on the clock period is that t_{CLOCK} has to be greater than or equal to t_{PD} of the register plus t_{PD} of the logic plus t_{SETUP} of the register. Plugging in the given timing parameters, we find that t_{CLOCK} must be greater than or equal to 5 plus 3 plus 2, which equals 10 nanoseconds.

Next, we want to determine what are the smallest setup and whole time specifications on the input in with respect to the active edge of the clock so that we can ensure that the necessary timing specifications are met. The IN input must be stable and valid long enough before the rising clock edge for it to propagate through the combinational logic and arrive at the register in time for it to setup. So t_{SETUP} of IN is greater than or equal to $t_{\text{PROPAGATION DELAY}}$ of the LOGIC plus t_{SETUP} of the register. That equals 3 plus 2, which equals 5 nanoseconds.

Once the IN input becomes invalid, the input to the register will become invalid after the contamination delay of the logic. IN must stay valid long enough to ensure that the input to the register does not become invalid before the registers hold time. So t_{HOLD} of IN plus t_{CD} of the LOGIC are greater than or equal to t_{HOLD} of the register. This can be rewritten as t_{HOLD} of IN must be greater than or equal to t_{HOLD} of the register minus t_{CD} of the LOGIC, which equals 0.3 minus 0.2. And that equals 0.1 nanoseconds.